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CORPORATE RESEARCH AND DEVELOPMENT GROUP

SPECIFICATION

MODEL No.

DEVICE SPECIFICATION FOR

TFT-LCD Open Cell

JE695R3HC2L

CUSTOMER'S APPROVAL

DATE _____

BY _____

Title & Department _____

Company _____

PRESENTED

BY 

Y. Minakuchi
Unit General Manager
Development Center
Corporate Research and Development Group
Sakai Display Products Corporation

RECORDS OF REVISION

MODEL No. : JE695R3HC2L

SPEC No. : LD-S18Y15

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-S18Y15	Nov. 26. 2018	-	-		1st ISSUE

1.1. Application

This specification applies to the color TFT-LCD Open-Cell "JE695R3HC2L".

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* In case of using the device for applications such as control and safety equipment for transportation (aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

*This products have been developed and are produced for Audio & Visual equipment.

* Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.

* SDP assumes no responsibility for any damage resulting from the use of the device that does not comply with the instructions and the precautions specified in these technical literature.

* Contact and consult with a SDP sales representative for any questions about this device.

2. Overview

This Open Cell (JE695R3HC2L) is a color active matrix LCD Open Cell incorporating amorphous silicon TFT (Thin Film Transistor), Polarizers, Source-PWBs, Source-Drivers, and Gate-Drivers made arrayed in glass BM area. The following content can be achieved in using C-PWB (JE0DZ1C0435) that SDP specifies. Graphics and texts can be displayed on a 3840 x RGB x 2160 dots panel with one billion colors (RGB 8bits + FRC) by using mini-LVDS (mini-Low Voltage Differential Signaling) to interface, +12.0V of DC supply voltages.

This Open Cell is designed for the Single Frame Rate driving. It can be displayed the moving picture smoothly to apply the Over Shoot driving (O/S driving) technology for the control circuit. In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.
With combination of these technologies, motion blur can be reduced and clearer display performance can be realized.
[Caution] You should design thermal conductive interface pad and C-PWB cover enough to radiate heat from IC in Source-Drivers and mounted parts on C-PWB.

This Open-Cell has below features.

- 4K2K (3840 x BGR x 2160) High Resolution
- VNB (Very Narrow Bezel) amorphous-silicon-TFT-LCD-Panel
- UV2A High Contrast and Transmittance Pixel Aperture
- Gate on array (GOA) structure
- Bezel-less processing for full flat TV design
- Wide-View angle with MPD (Multi-Pixel-Driving)
- High-Speed-mini-LVDS Driver Interface Technology for V-by-One® HS control system with the Special C-PWB: JE0DZ1C0435"

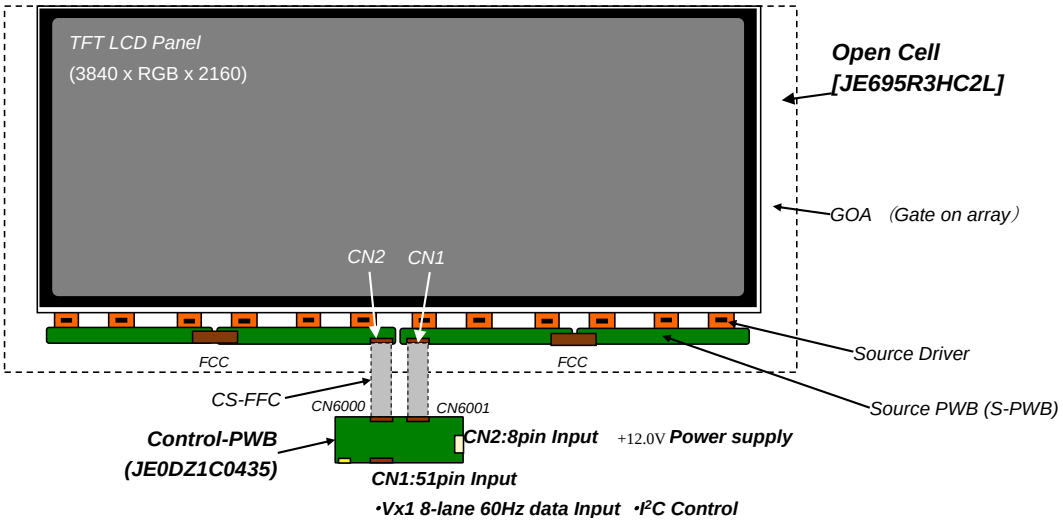


Fig.1 Diagram of the Open Cell and C-PWB

3. Mechanical Specifications

Parameter	Specification	Unit
Display size (Active Area)	1535.232 (H) x 871.560 (V) 176.538 (Diagonal) [69.5”]	mm cm
Pixel Format	3840 (H) x 2160 (V) (1pixel = R + G + B dot)	pixel
Pixel pitch	0.3998(H) x 0.3998 (V)	mm
Pixel configuration	B,G,R vertical stripe	-
Display mode	Normally black	-
Outline dimensions [1)]	1545.232 (H) x 929.96 (V) x 4.0 (D)	mm
Mass	4.4±0.3	kg
Surface treatment [2)]	- Front polarizer: Low-Haze(less than 5%) Anti-Glare, Hard-Coating(2H and more) - Rear polarizer: Hard-Coating less	-

1) The thickest point is the 96pin-CN on the S-PWB, the display area thickness is shown the outline drawing in Page 19.
2) With the protection film removed.

4. Driving System Specifications (with C-PWB “JE0DZ1C0435”)

4.1 Input Interface Specifications

CN2 of the C-PWB “JE0DZ1C0435”: +12.0V Power Supply

- Using Connector : A2010WR0-8PS-SHP (JWT)
- Mating Connector : A2010H00-8P-SHP (JWT)

Pin No.	CN2 of C-PWB “JE0DZ1C0435”	
	Pin Name	Signal
1	VCC	Power Supply (+12.0V DC)
2	VCC	Power Supply (+12.0V DC)
3	VCC	Power Supply (+12.0V DC)
4	VCC	Power Supply (+12.0V DC)
5	NC	-
6	GND	GND
7	GND	GND
8	GND	GND

CN1 of C-PWB “JE0DZ1C0435”: Vx1_8-Lane_Data and I^2C Control

- Using Connector : FI-RTE51SZ-HF (JAE)
- Mating Connector : FI-RE51HL, FI-RE51CL (JAE) or Equivalent Connector
- Mating V-by-One® HS Transmitter : THCV215 (THine) or Equivalent Device

Pin No.	CN1 of C-PWB “JE0DZ1C0435”		
	Pin Name	Signal	Remark
1	VCC	Power Supply	+12.0V
2	VCC	Power Supply	+12.0V
3	VCC	Power Supply	+12.0V
4	VCC	Power Supply	+12.0V
5	VCC	Power Supply	+12.0V
6	VCC	Power Supply	+12.0V
7	VCC	Power Supply	+12.0V
8	VCC	Power Supply	+12.0V
9	NC	-	Open
10	GND	GND	
11	GND	GND	
12	GND	GND	
13	GND	GND	
14	GND	GND	
15	NC	-	Open
16	NC	-	Open
17	NC	-	Open
18	I2C_SDA	I^2C Data	Pull-Up (3.3 V) [1)]
19	I2C_SCL	I^2C Clock	Pull-Up (3.3 V) [1)]
20	NC	-	Open
21	NC	-	Open
22	NC	-	Open
23	NC	-	Open
24	NC	-	Open
25	HTPDN	Hot Plug Detect Output	L : Active and Connection Hi-Z : Inactive and No Connection (Open Drain) [2)]
26	LOCKN	Lock Detect Output	L : Lock / Hi-Z : Unlock (Open Drain) [2)]
27	CML GND	GND	

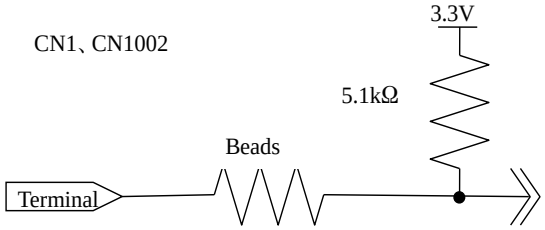
28	Rx0n	Vx1 Input Data_Lane-0	3)
29	Rx0p	Vx1 Input Data_Lane-0	3)
30	CML GND	GND	
31	Rx1n	Vx1 Input Data_Lane-1	3)
32	Rx1p	Vx1 Input Data_Lane-1	3)
33	CML GND	GND	
34	Rx2n	Vx1 Input Data_Lane-2	3)
35	Rx2p	Vx1 Input Data_Lane-2	3)
36	CML GND	GND	
37	Rx3n	Vx1 Input Data_Lane-3	3)
38	Rx3p	Vx1 Input Data_Lane-3	3)
39	CML GND	GND	
40	Rx4n	Vx1 Input Data_Lane-4	3)
41	Rx4p	Vx1 Input Data_Lane-4	3)
42	CML GND	GND	
43	Rx5n	Vx1 Input Data_Lane-5	3)
44	Rx5p	Vx1 Input Data_Lane-5	3)
45	CML GND	GND	
46	Rx6n	Vx1 Input Data_Lane-6	3)
47	Rx6p	Vx1 Input Data_Lane-6	3)
48	CML GND	GND	
49	Rx7n	Vx1 Input Data_Lane-7	3)
50	Rx7p	Vx1 Input Data_Lane-7	3)
51	CML GND	GND	

CN1002 of C-PWB "JE0DZ1C0435": I²C Control

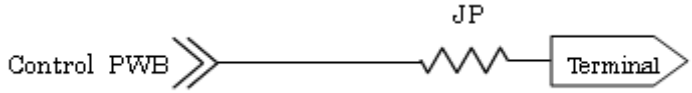
- Interface Type : 1.5mm-pitch/0.75mm-phi Via Hole
- Mating Connector : [Housing]5P-SZN(JST)
  [Contact]SZN-002T-P0.7K (JST) or Equivalent Connector

Pin No.	CN1002 of C-PWB "JE0DZ1C0435"		
	Pin Name	Signal	Remark
1	SCL	I²C Clock	Pull-Up (3.3 V) 1)
2	SDA	I²C Data	Pull-Up (3.3 V) 1)
3	(Reserved)	-	(Non-Connection)
4	NC	-	No via hole
5	GND	GND	

1) The equivalent circuit for the terminal of I2C_SDA, I2C_SCL , SCL, SDA.



2) The equivalent circuit for the terminal of HTPDN, LOCKN.



3) (a) V-by-One® HS _ Byte Length and Color Data Mapping

Byte	Packer Input	Color Data Mapping
Byte 0	D[0]	R2
	D[1]	R3
	D[2]	R4
	D[3]	R5
	D[4]	R6
	D[5]	R7
	D[6]	R8
	D[7]	R9(MSB)
Byte 1	D[8]	G2
	D[9]	G3
	D[10]	G4
	D[11]	G5
	D[12]	G6
	D[13]	G7
	D[14]	G8
	D[15]	G9(MSB)
Byte 2	D[16]	B2
	D[17]	B3
	D[18]	B4
	D[19]	B5
	D[20]	B6
	D[21]	B7
	D[22]	B8
	D[23]	B9(MSB)
Byte 3	D[24]	-
	D[25]	-
	D[26]	B0(LSB)
	D[27]	B1
	D[28]	G0(LSB)
	D[29]	G1
	D[30]	R0(LSB)
	D[31]	R1

(b)Mini-LVDS Mapping

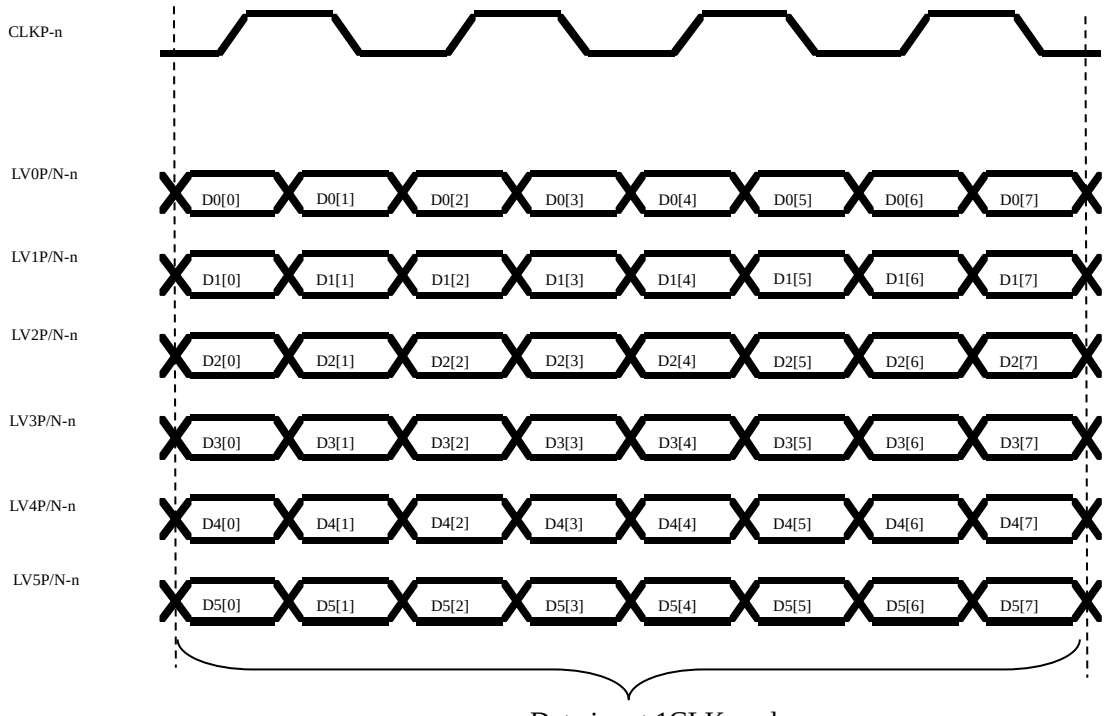


Fig.2 mini-LVDS Mapping

(c) Display data composition

MSB							LSB
Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]

n=0～5

(d) Display data and output

SSOF1、2、3、4、5、6

Display data	D5[0] ～D5[7]	D4[0] ～D4[7]	D3[0] ～D3[7]	D2[0] ～D2[7]	・・・・・・	D2[0] ～D2[7]	D1[0] ～D1[7]	D0[0] ～D0[7]
Output	S960	S959	S958	S957	・・・・・・	S3	S2	S1

SSOF7、8、9、10、11、12

Display data	D0[0] ～D0[7]	D1[0] ～D1[7]	D2[0] ～D2[7]	D3[0] ～D3[7]	・・・・・・	D3[0] ～D3[7]	D4[0] ～D4[7]	D5[0] ～D5[7]
Output	S1	S2	S3	S4	・・・・・・	S958	S959	S960

(e) The scan direction is setting for using S-PWBs' side down.

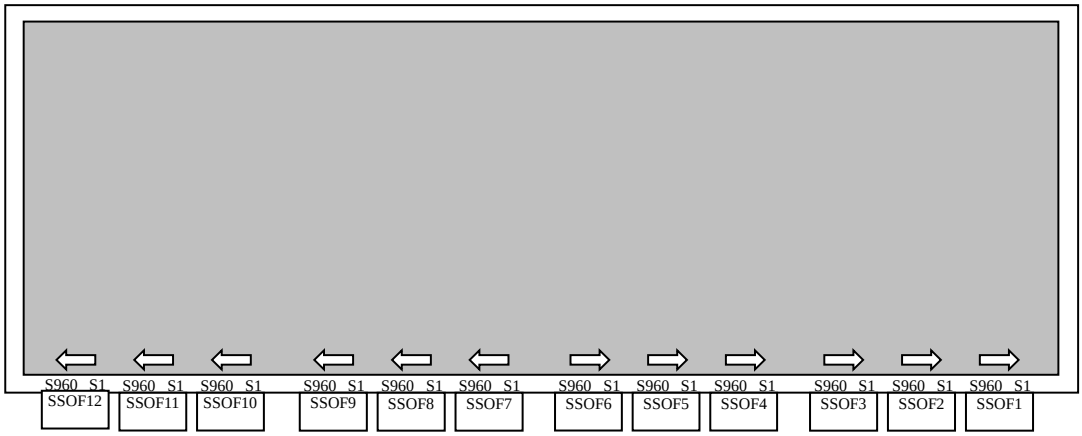
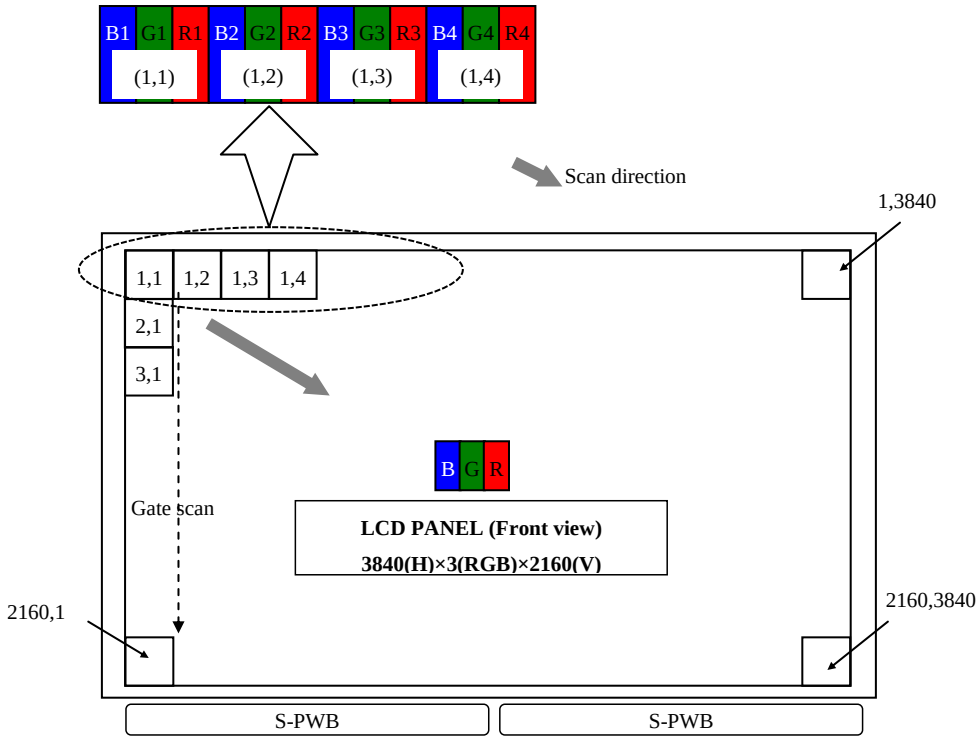


Fig.3 Scan direction

(f) Display direction & PWB layout

In this module each subpixel R, G, B is aligned as follows. Two S-PWBs are layout at the bottom side of the screen.



LCD subpixel alignment

Fig.4 Input data signal and display position on the screen

4.2. Connection between C-PWB "JE0DZ1C0435" and S-PWB

CN3 and CN4 of C-PWB "JE0DZ1C0435" → CN2 and CN1 of S-PWB

- C-PWB Output Connector (CN6000,CN6001) : 04 6815 096 010 846+ (KYOCERA) or Equivalent Connector
- S-PWB Input Connector (CN2,1) : 04 6815 096 010 846+ (KYOCERA) or Equivalent Connector
- Recommended Terminal Figure of FFC or FPC :

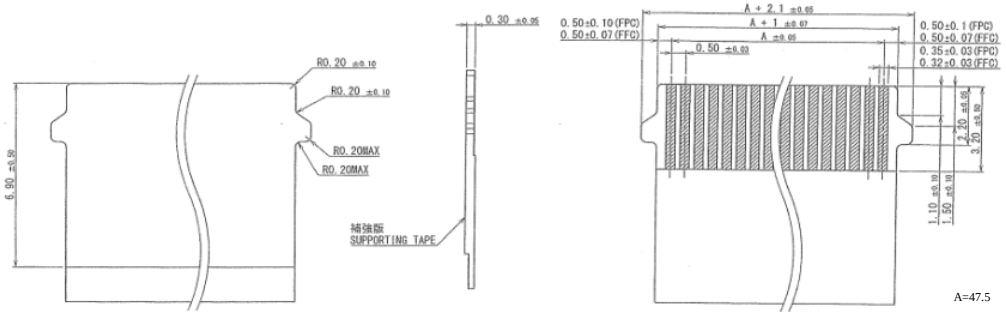


Fig.5 Recommended Terminal Figure of FFC or FPC

[Note] Contact SDP or the connector manufacturer for details of the FFC or FPC design.

Output : CN6000 of C-PWB "JE0DZ1C0435"			Input : CN2 of S-PWB2		
Pin No.	Pin Name	Output Signal	Pin No.	Pin Name	Connected to
96	GND	GND	1	GND	GND
95	NC	OPEN	2	NC	OPEN
94	NC	OPEN	3	NC	OPEN
93	NC	OPEN	4	NC	OPEN
92	NC	OPEN	5	NC	OPEN
91	GND	GND	6	GND	GND
90	NC	OPEN	7	NC	OPEN
89	VSS1	Gate Low Power Supply	8	VSS1	Gate Low Power Supply
88	VSS2	Gate Low Power Supply	9	VSS2	Gate Low Power Supply
87	NC	OPEN	10	NC	OPEN
86	GSP1	Gate Start Pulse	11	GSP1	Gate Start Pulse
85	GSP2	OPEN	12	GSP2	OPEN
84	GSP3	OPEN	13	GSP3	OPEN
83	GCK1	Gate Clock 1	14	GCK1	Gate Clock 1
82	GCK2	Gate Clock 2	15	GCK2	Gate Clock 2
81	GCK3	Gate Clock 3	16	GCK3	Gate Clock 3
80	GCK4	Gate Clock 4	17	GCK4	Gate Clock 4
79	GCK5	Gate Clock 5	18	GCK5	Gate Clock 5
78	GCK6	Gate Clock 6	19	GCK6	Gate Clock 6
77	GCK7	Gate Clock 7	20	GCK7	Gate Clock 7
76	GCK8	Gate Clock 8	21	GCK8	Gate Clock 8
75	CLR	OPEN	22	CLR	OPEN
74	GEP1	Gate End Pulse	23	GEP1	Gate End Pulse
73	GEP2	OPEN	24	GEP2	OPEN
72	GEP3	OPEN	25	GEP3	OPEN
71	GEP4	OPEN	26	GEP4	OPEN
70	NC	OPEN	27	NC	OPEN
69	GND	GND	28	GND	GND
68	LV5N-4	mini-LVDS Differential Data (LV5N-4)	29	LV5N-4	mini-LVDS Differential Data (LV5N-4)
67	LV5P-4	mini-LVDS Differential Data (LV5P-4)	30	LV5P-4	mini-LVDS Differential Data (LV5P-4)
66	LV4N-4	mini-LVDS Differential Data (LV4N-4)	31	LV4N-4	mini-LVDS Differential Data (LV4N-4)
65	LV4P-4	mini-LVDS Differential Data (LV4P-4)	32	LV4P-4	mini-LVDS Differential Data (LV4P-4)
64	LV3N-4	mini-LVDS Differential Data (LV3N-4)	33	LV3N-4	mini-LVDS Differential Data (LV3N-4)
63	LV3P-4	mini-LVDS Differential Data (LV3P-4)	34	LV3P-4	mini-LVDS Differential Data (LV3P-4)
62	GND	GND	35	GND	GND
61	CLKN-4	mini-LVDS Differential Clock (LVCLKN-4)	36	CLKN-4	mini-LVDS Differential Clock (LVCLKN-4)
60	CLKP-4	mini-LVDS Differential Clock (LVCLKP-4)	37	CLKP-4	mini-LVDS Differential Clock (LVCLKP-4)
59	GND	GND	38	GND	GND
58	LV2N-4	mini-LVDS Differential Data (LV2N-4)	39	LV2N-4	mini-LVDS Differential Data (LV2N-4)
57	LV2P-4	mini-LVDS Differential Data (LV2P-4)	40	LV2P-4	mini-LVDS Differential Data (LV2P-4)
56	LV1N-4	mini-LVDS Differential Data (LV1N-4)	41	LV1N-4	mini-LVDS Differential Data (LV1N-4)
55	LV1P-4	mini-LVDS Differential Data (LV1P-4)	42	LV1P-4	mini-LVDS Differential Data (LV1P-4)
54	LV0N-4	mini-LVDS Differential Data (LV0N-4)	43	LV0N-4	mini-LVDS Differential Data (LV0N-4)
53	LV0P-4	mini-LVDS Differential Data (LV0P-4)	44	LV0P-4	mini-LVDS Differential Data (LV0P-4)
52	GND	GND	45	GND	GND
51	LV5N-3	mini-LVDS Differential Data (LV5N-3)	46	LV5N-3	mini-LVDS Differential Data (LV5N-3)
50	LV5P-3	mini-LVDS Differential Data (LV5P-3)	47	LV5P-3	mini-LVDS Differential Data (LV5P-3)
49	LV4N-3	mini-LVDS Differential Data (LV4N-3)	48	LV4N-3	mini-LVDS Differential Data (LV4N-3)
48	LV4P-3	mini-LVDS Differential Data (LV4P-3)	49	LV4P-3	mini-LVDS Differential Data (LV4P-3)
47	LV3N-3	mini-LVDS Differential Data (LV3N-3)	50	LV3N-3	mini-LVDS Differential Data (LV3N-3)
46	LV3P-3	mini-LVDS Differential Data (LV3P-3)	51	LV3P-3	mini-LVDS Differential Data (LV3P-3)
45	GND	GND	52	GND	GND
44	CLKN-3	mini-LVDS Differential Clock (LVCLKN-3)	53	CLKN-3	mini-LVDS Differential Clock (LVCLKN-3)
43	CLKP-3	mini-LVDS Differential Clock (LVCLKP-3)	54	CLKP-3	mini-LVDS Differential Clock (LVCLKP-3)
42	GND	GND	55	GND	GND

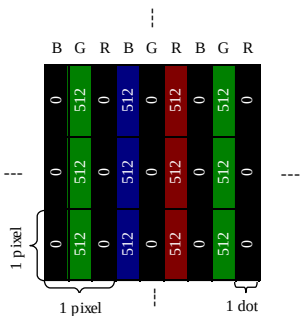
41	LV2N-3	mini-LVDS Differential Data (LV2N-3)	56	LV2N-3	mini-LVDS Differential Data (LV2N-3)
40	LV2P-3	mini-LVDS Differential Data (LV2P-3)	57	LV2P-3	mini-LVDS Differential Data (LV2P-3)
39	LV1N-3	mini-LVDS Differential Data (LV1N-3)	58	LV1N-3	mini-LVDS Differential Data (LV1N-3)
38	LV1P-3	mini-LVDS Differential Data (LV1P-3)	59	LV1P-3	mini-LVDS Differential Data (LV1P-3)
37	LV0N-3	mini-LVDS Differential Data (LV0N-3)	60	LV0N-3	mini-LVDS Differential Data (LV0N-3)
36	LV0P-3	mini-LVDS Differential Data (LV0P-3)	61	LV0P-3	mini-LVDS Differential Data (LV0P-3)
35	GND	GND	62	GND	GND
34	LS	Source-Driver Latch Pulse	63	LS	Source-Driver Latch Pulse
33	REV	Source Output Polarity Control	64	REV	Source Output Polarity Control
32	FS	Source-Driver control signal	65	FS	Source-Driver control signal
31	GND	GND	66	GND	GND
30	VL255	Gamma Reference Voltage	67	VL255	Gamma Reference Voltage
29	VL247	Gamma Reference Voltage	68	VL247	Gamma Reference Voltage
28	VL191	Gamma Reference Voltage	69	VL191	Gamma Reference Voltage
27	VL127	Gamma Reference Voltage	70	VL127	Gamma Reference Voltage
26	VL63	Gamma Reference Voltage	71	VL63	Gamma Reference Voltage
25	VL31	Gamma Reference Voltage	72	VL31	Gamma Reference Voltage
24	VL0	Gamma Reference Voltage	73	VL0	Gamma Reference Voltage
23	HVDD	Source driver analog voltage	74	HVDD	Source driver analog voltage
22	VH0	Gamma Reference Voltage	75	VH0	Gamma Reference Voltage
21	VH31	Gamma Reference Voltage	76	VH31	Gamma Reference Voltage
20	VH63	Gamma Reference Voltage	77	VH63	Gamma Reference Voltage
19	VH127	Gamma Reference Voltage	78	VH127	Gamma Reference Voltage
18	VH191	Gamma Reference Voltage	79	VH191	Gamma Reference Voltage
17	VH247	Gamma Reference Voltage	80	VH247	Gamma Reference Voltage
16	VH255	Gamma Reference Voltage	81	VH255	Gamma Reference Voltage
15	NC	OPEN	82	NC	OPEN
14	GND	GND	83	GND	GND
13	VCC_ 3.3V	S-IC_VCC & Pull-Up-Line	84	VCC_3.3V	S-IC_VCC & Pull-Up-Line
12	VCC_3.3V	S-IC_VCC & Pull-Up-Line	85	VCC_3.3V	S-IC_VCC & Pull-Up-Line
11	NC	OPEN	86	NC	OPEN
10	VLS	Source Driver Power Voltage	87	VLS	Source Driver Power Voltage
9	VLS	Source Driver Power Voltage	88	VLS	Source Driver Power Voltage
8	VLS	Source Driver Power Voltage	89	VLS	Source Driver Power Voltage
7	VLS	Source Driver Power Voltage	90	VLS	Source power supply
6	NC	NC	91	NC	NC
5	VCOM	TFT-LCD-Panel Common Voltage [1)]	92	VCOM	TFT-LCD-Panel Common Voltage [1)]
4	VCOM	TFT-LCD-Panel Common Voltage [1)]	93	VCOM	TFT-LCD-Panel Common Voltage [1)]
3	CS	OPEN	94	CS	OPEN
2	NC	OPEN	95	NC	OPEN
1	GND	GND	96	GND	GND

Output : CN6001 of C-PWB “JE0DZ1C0435”					
Pin No.	Pin Name	Output Signal	Pin No.	Pin Name	Connected to
96	GND	GND	1	GND	GND
95	NC	OPEN	2	NC	OPEN
94	CS	OPEN	3	CS	OPEN
93	VCOM	TFT-LCD-Panel Common Voltage [1)]	4	VCOM	TFT-LCD-Panel Common Voltage [1)]
92	VCOM	TFT-LCD-Panel Common Voltage [1)]	5	VCOM	TFT-LCD-Panel Common Voltage [1)]
91	NC	OPEN	6	NC	
90	VLS	Source Driver Power Voltage	7	VLS	Source Driver Power Voltage
89	VLS	Source Driver Power Voltage	8	VLS	Source Driver Power Voltage
88	VLS	Source Driver Power Voltage	9	VLS	Source Driver Power Voltage
87	VLS	Source Driver Power Voltage	10	VLS	Source Driver Power Voltage
86	NC	OPEN	11	NC	OPEN
85	VCC_ 3.3V	S-IC_VCC & Pull-Up-Line	12	VCC_ 3.3V	S-IC_VCC & Pull-Up-Line
84	VCC_3.3V	S-IC_VCC & Pull-Up-Line	13	VCC_3.3V	S-IC_VCC & Pull-Up-Line
83	GND	GND	14	GND	GND
82	VL255	Gamma Reference Voltage	15	VL255	Gamma Reference Voltage
81	VL247	Gamma Reference Voltage	16	VL247	Gamma Reference Voltage
80	VL191	Gamma Reference Voltage	17	VL191	Gamma Reference Voltage
79	VL127	Gamma Reference Voltage	18	VL127	Gamma Reference Voltage
78	VL63	Gamma Reference Voltage	19	VL63	Gamma Reference Voltage
77	VL31	Gamma Reference Voltage	20	VL31	Gamma Reference Voltage
76	VL0	Gamma Reference Voltage	21	VL0	Gamma Reference Voltage
75	HVDD	Source driver analog voltage	22	HVDD	Source driver analog voltage
74	VH0	Gamma Reference Voltage	23	VH0	Gamma Reference Voltage
73	VH31	Gamma Reference Voltage	24	VH31	Gamma Reference Voltage
72	VH63	Gamma Reference Voltage	25	VH63	Gamma Reference Voltage
71	VH127	Gamma Reference Voltage	26	VH127	Gamma Reference Voltage
70	VH191	Gamma Reference Voltage	27	VH191	Gamma Reference Voltage
69	VH247	Gamma Reference Voltage	28	VH247	Gamma Reference Voltage
68	VH255	Gamma Reference Voltage	29	VH255	Gamma Reference Voltage
67	NC	OPEN	30	NC	OPEN
66	GND	GND	31	GND	GND
65	FS	Source-Driver control signal	32	FS	Source-Driver control signal
64	REV	Source Output Polarity Control	33	REV	Source Output Polarity Control
63	LS	Source-Driver Latch Pulse	34	LS	Source-Driver Latch Pulse
62	GND	GND	35	GND	GND

61	LV5N-2	mini-LVDS Differential Data (LV5N-2)	36	LV5N-2	mini-LVDS Differential Data (LV5N-2)
60	LV5P-2	mini-LVDS Differential Data (LV5P-2)	37	LV5P-2	mini-LVDS Differential Data (LV5P-2)
59	LV4N-2	mini-LVDS Differential Data (LV4N-2)	38	LV4N-2	mini-LVDS Differential Data (LV4N-2)
58	LV4P-2	mini-LVDS Differential Data (LV4P-2)	39	LV4P-2	mini-LVDS Differential Data (LV4P-2)
57	LV3N-2	mini-LVDS Differential Data (LV3N-2)	40	LV3N-2	mini-LVDS Differential Data (LV3N-2)
56	LV3P-2	mini-LVDS Differential Data (LV3P-2)	41	LV3P-2	mini-LVDS Differential Data (LV3P-2)
55	GND	GND	42	GND	GND
54	CLKN-2	mini-LVDS Differential Clock (LVCLKN-2)	43	CLKN-2	mini-LVDS Differential Clock (LVCLKN-2)
53	CLKP-2	mini-LVDS Differential Clock (LVCLKP-2)	44	CLKP-2	mini-LVDS Differential Clock (LVCLKP-2)
52	GND	GND	45	GND	GND
51	LV2N-2	mini-LVDS Differential Data (LV2N-2)	46	LV2N-2	mini-LVDS Differential Data (LV2N-2)
50	LV2P-2	mini-LVDS Differential Data (LV2P-2)	47	LV2P-2	mini-LVDS Differential Data (LV2P-2)
49	LV1N-2	mini-LVDS Differential Data (LV1N-2)	48	LV1N-2	mini-LVDS Differential Data (LV1N-2)
48	LV1P-2	mini-LVDS Differential Data (LV1P-2)	49	LV1P-2	mini-LVDS Differential Data (LV1P-2)
47	LV0N-2	mini-LVDS Differential Data (LV0N-2)	50	LV0N-2	mini-LVDS Differential Data (LV0N-2)
46	LV0P-2	mini-LVDS Differential Data (LV0P-2)	51	LV0P-2	mini-LVDS Differential Data (LV0P-2)
45	GND	GND	52	GND	GND
44	LV5N-1	mini-LVDS Differential Data (LV5N-1)	53	LV5N-1	mini-LVDS Differential Data (LV5N-1)
43	LV5P-1	mini-LVDS Differential Data (LV5P-1)	54	LV5P-1	mini-LVDS Differential Data (LV5P-1)
42	LV4N-1	mini-LVDS Differential Data (LV4N-1)	55	LV4N-1	mini-LVDS Differential Data (LV4N-1)
41	LV4P-1	mini-LVDS Differential Data (LV4P-1)	56	LV4P-1	mini-LVDS Differential Data (LV4P-1)
40	LV3N-1	mini-LVDS Differential Data (LV3N-1)	57	LV3N-1	mini-LVDS Differential Data (LV3N-1)
39	LV3P-1	mini-LVDS Differential Data (LV3P-1)	58	LV3P-1	mini-LVDS Differential Data (LV3P-1)
38	GND	GND	59	GND	GND
37	CLKN-1	mini-LVDS Differential Data (LVCLKN-1)	60	CLKN-1	mini-LVDS Differential Data (LVCLKN-1)
36	CLKP-1	mini-LVDS Differential Data (LVCLKP-1)	61	CLKP-1	mini-LVDS Differential Data (LVCLKP-1)
35	GND	GND	62	GND	GND
34	LV2N-1	mini-LVDS Differential Data (LV2N-1)	63	LV2N-1	mini-LVDS Differential Data (LV2N-1)
33	LV2P-1	mini-LVDS Differential Data (LV2P-1)	64	LV2P-1	mini-LVDS Differential Data (LV2P-1)
32	LV1N-1	mini-LVDS Differential Data (LV1N-1)	65	LV1N-1	mini-LVDS Differential Data (LV1N-1)
31	LV1P-1	mini-LVDS Differential Data (LV1P-1)	66	LV1P-1	mini-LVDS Differential Data (LV1P-1)
30	LV0N-1	mini-LVDS Differential Data (LV0N-1)	67	LV0N-1	mini-LVDS Differential Data (LV0N-1)
29	LV0P-1	mini-LVDS Differential Data (LV0P-1)	68	LV0P-1	mini-LVDS Differential Data (LV0P-1)
28	GND	GND	69	GND	GND
27	NC	OPEN	70	NC	OPEN
26	GEP4	OPEN	71	GEP4	OPEN
25	GEP3	OPEN	72	GEP3	OPEN
24	GEP2	OPEN	73	GEP2	OPEN
23	GEP1	Gate End Pulse	74	GEP1	Gate End Pulse
22	CLR	OPEN	75	CLR	OPEN
21	GCK8	Gate Clock 8	76	GCK8	Gate Clock 8
20	GCK7	Gate Clock 7	77	GCK7	Gate Clock 7
19	GCK6	Gate Clock 6	78	GCK6	Gate Clock 6
18	GCK5	Gate Clock 5	79	GCK5	Gate Clock 5
17	GCK4	Gate Clock 4	80	GCK4	Gate Clock 4
16	GCK3	Gate Clock 3	81	GCK3	Gate Clock 3
15	GCK2	Gate Clock 2	82	GCK2	Gate Clock 2
14	GCK1	Gate Clock 1	83	GCK1	Gate Clock 1
13	GSP3	OPEN	84	GSP3	OPEN
12	GSP2	OPEN	85	GSP2	OPEN
11	GSP1	Gate Start Pulse	86	GSP1	Gate Start Pulse
10	NC	OPEN	87	NC	OPEN
9	VSS2	Gate Low Power Supply	88	VSS2	Gate Low Power Supply
8	VSS1	Gate Low Power Supply	89	VSS1	Gate Low Power Supply
7	NC	OPEN	90	NC	OPEN
6	GND	GND	91	GND	GND
5	(Reserved)	(SPI-FLASH Control)	92	(Reserved)	(SPI-FLASH Control)
4	(Reserved)	(SPI-FLASH Control)	93	(Reserved)	(SPI-FLASH Control)
3	(Reserved)	(SPI-FLASH Control)	94	(Reserved)	(SPI-FLASH Control)
2	(Reserved)	(SPI-FLASH Control)	95	(Reserved)	(SPI-FLASH Control)
1	GND	GND	96	GND	GND

1) For the prevention of a long-time image sticking of the TFT-LCD panel, be sure to offset the Common Voltage (Vcom) for each panel.

<Vcom Tuning Pattern: 1-Source-Line-Stripe>



4.3. Absolute Maximum Ratings (with C-PWB "JE0DZ1C0435")

(GND = 0 V)

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input Power Voltage	VCC	Ta = 25ºC	0 to +15.2	V	C-PWB : VCC
Input Control Voltage	V_I	Ta = 25ºC	-0.3 to +3.6	V	C-PWB : I2C_SDA, I2C_SCL, HTPDN, LOCKN, SCL, SDA
Input Vx1 Data Voltage	V_{VBO}	Ta = 25ºC	-0.3 to +3.0	V	C-PWB : Rx*n/p
Storage Temperature	Tstg	-	-20 to +60	ºC	Open-Cell with C-PWB
Operation Temperature	Topa	-	0 to +50	ºC	Open-Cell with C-PWB [1)]

- Humidity 95%RH Max.(at Ta ≦ 40 ºC)
- Maximum wet-bulb temperature 39 ºC or less (at Ta > 40 ºC)
- No condensation.
- Design the module with a maintaining temperature of the panel at 60ºC or less and uniform as much as possible. Otherwise there is possibility to cause several issues such as "Mura" or "Gamma shift", etc.
- Design the module with a maintaining temperature of Black Mask(BM) area of panel at 70 ºC or less and uniform as much as possible. Otherwise there is possibility to cause functional issue in GOA circuit, which is located at BM area.

1) Refer to the C-PWB's Specification(LD-S18Y12) for the operation temperature of ICs on the C-PWB.
2) The recommended operating maximum temperature of the Source-Driver-IC is 125 ºC at a chip surface.

4.4. Electrical Characteristics of Input Signals (with C-PWB "JE0DZ1C0435")

(Ta = 25 ºC)

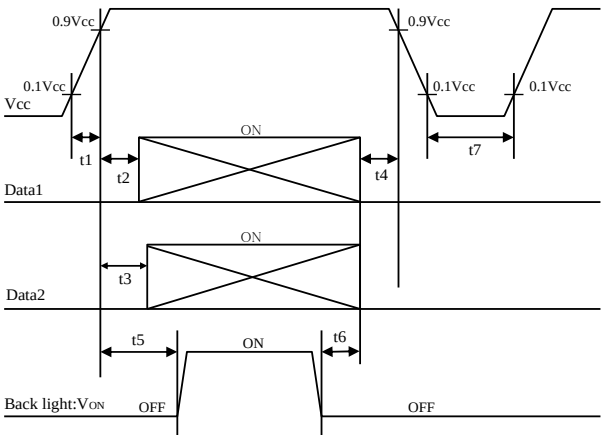
Item		Symbol	Min.	Typ.	Max.	Unit	Note
C-PWB Power	Supply Voltage [1)]	VCC	10.8	12.0	13.2	V	
	Current Dissipation [2)]	ICC	-	0.74	3.03	A	
	Inrush Current [3)]	Irush1	-	6.60	-	A	
		Irush2		7.61			
Permissible Input Ripple Voltage		V_{RP}	-	-	600	mVpp	
Differential Input High Threshold [4)]		V_{RTH}	-	-	50	mV	
Differential Input Low Threshold [4)]		V_{RTL}	-50	-	-	mV	
Unit Interval [4)]		UI	250	-	617	Ps	
Input Signal Rate [4)]		F_{bit}	2.68	2.97	3.13	Gbps	
Differential Input Allowable Intra-pair Skew [5)]		tRISK_INTRA	-	-	0.3	UI	
Differential Input Allowable Inter-pair Skew [5)]		tRISK_INTER	-	-	5	UI	
Input Low Voltage [6)]		V_{IL}	0	-	0.4	V	
Input High Voltage [6)]		V_{IH}	2.3	-	3.3	V	
Terminal Resistor		Rt	-	100	-	Ohm	Differential Input

- In any case, input voltage should not exceed the maximum level or should not be below the minimum level including any ripple.

1) Sequences of power and signals

Input voltage sequences

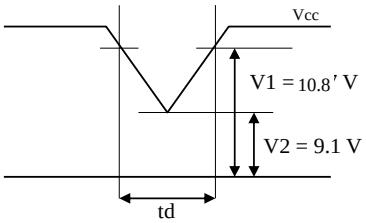
500 us < t1 < 20 ms
20 ms < t2
910 ms < t3
0 < t4 < 1 s
1 s < t5
0 < t6
1 s < t7



Dip condition for supply voltage

a) V2 ≦ VCC < V1
td < 10 ms

b) VCC < V2
This case is based on 'Input voltage sequences'.

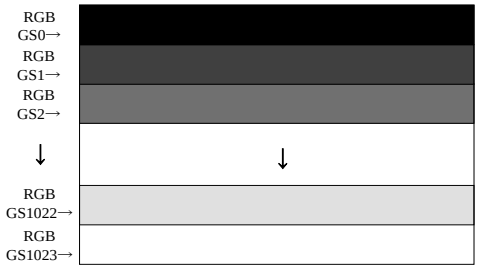


Data1 : Vx1 Differential Data (Rx*n/p)
Data2 : Control Signals (I2C_SDA, I2C_SCL)

When the back light is switched on before a panel operation or after a panel operation stop, it may not display normally. But this phenomenon is not based on change of an incoming signal, and does not give damage to a liquid crystal display.

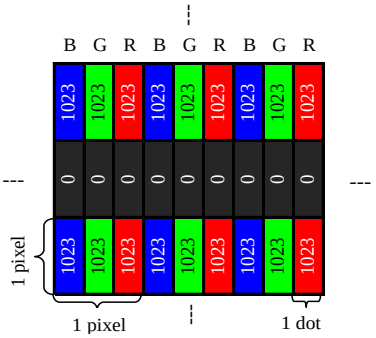
2) Definition Pattern of Current Dissipation

Typical Current Situation: 1024-Gray-Bar-Pattern

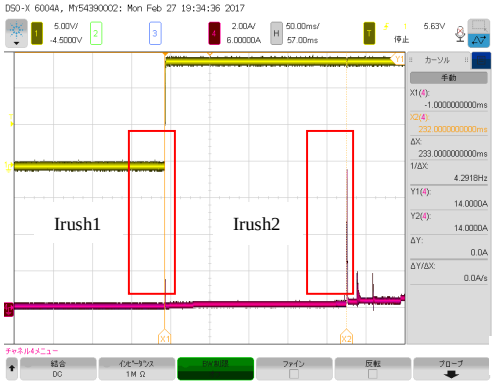


V_{CC} = +12.0V
1/Tc = 74.25 MHz
TH = 7.4 us
TV = 2250 (60 Hz)

Max Current Situation: 1-Gate-Line-Stripe



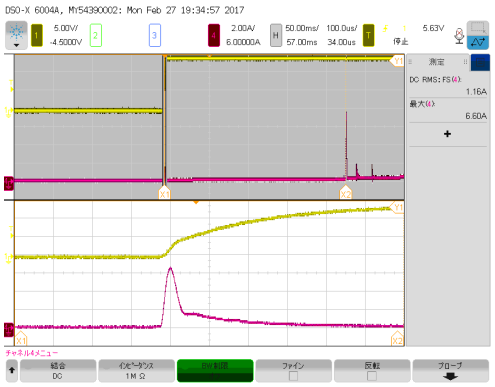
3) V_{CC} = +12.0V Inrush Current Waveform (Ref.t1=500usec)



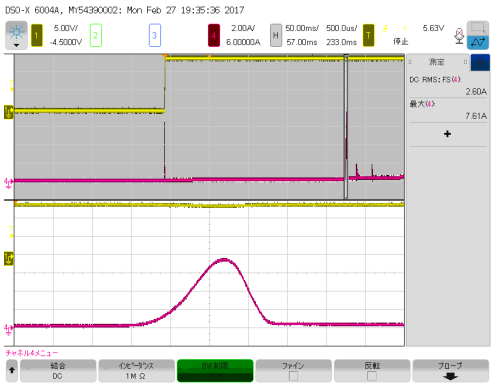
V_{CC}=+12.0V 5V/div

Irush 2A/div

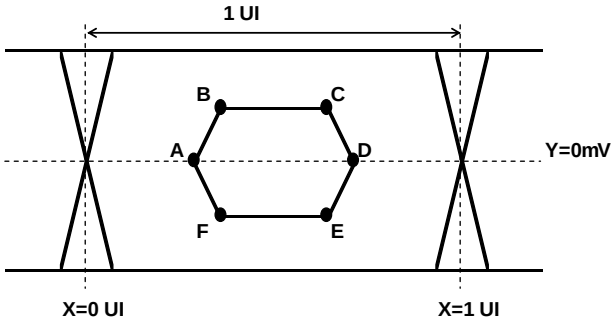
Irush1



Irush2

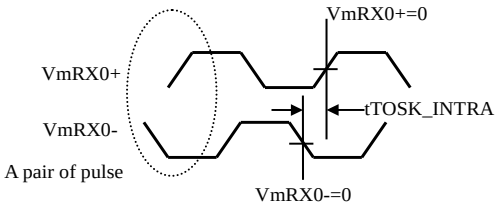


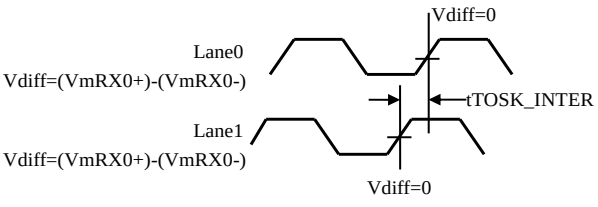
4) Eye Diagram (Eye Mask)



	X[UI]	Y[mV]
A	0.25	0
B	0.3	50
C	0.7	50
D	0.75	0
E	0.7	−50
F	0.3	−50

5)





6) Control Signals (I2C_SDA, I2C_SCL, HTPDN, LOCKN)

4.5. Timing Characteristics (with C-PWB “JE0DZ1C0435”)

Timing diagram of input signals is shown in below figure.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Clock	Frequency	1/Tc	67	74.25	78.25	MHz	
Data Enable Signal	Horizontal Period	TH	530	550	702	clock	
			7.07	7.41	-	µs	
	Horizontal Period (High)	THd	480	480	480	clock	
	Vertical Period	TV	2240	2250	2872	line	
			47	60	60.32	Hz	
	Vertical Period (High)	TVd	2160	2160	2160	line	

- When the vertical period is very long, flicker and etc. may occur.
- Turn off the module after it shows the black screen.
- Make sure that a length of vertical period should become of an integral multiple of a horizontal length of period. Otherwise, the screen may not display properly.
- As for your final setting of driving timing, we will conduct operation check test at our side, please inform your final setting.

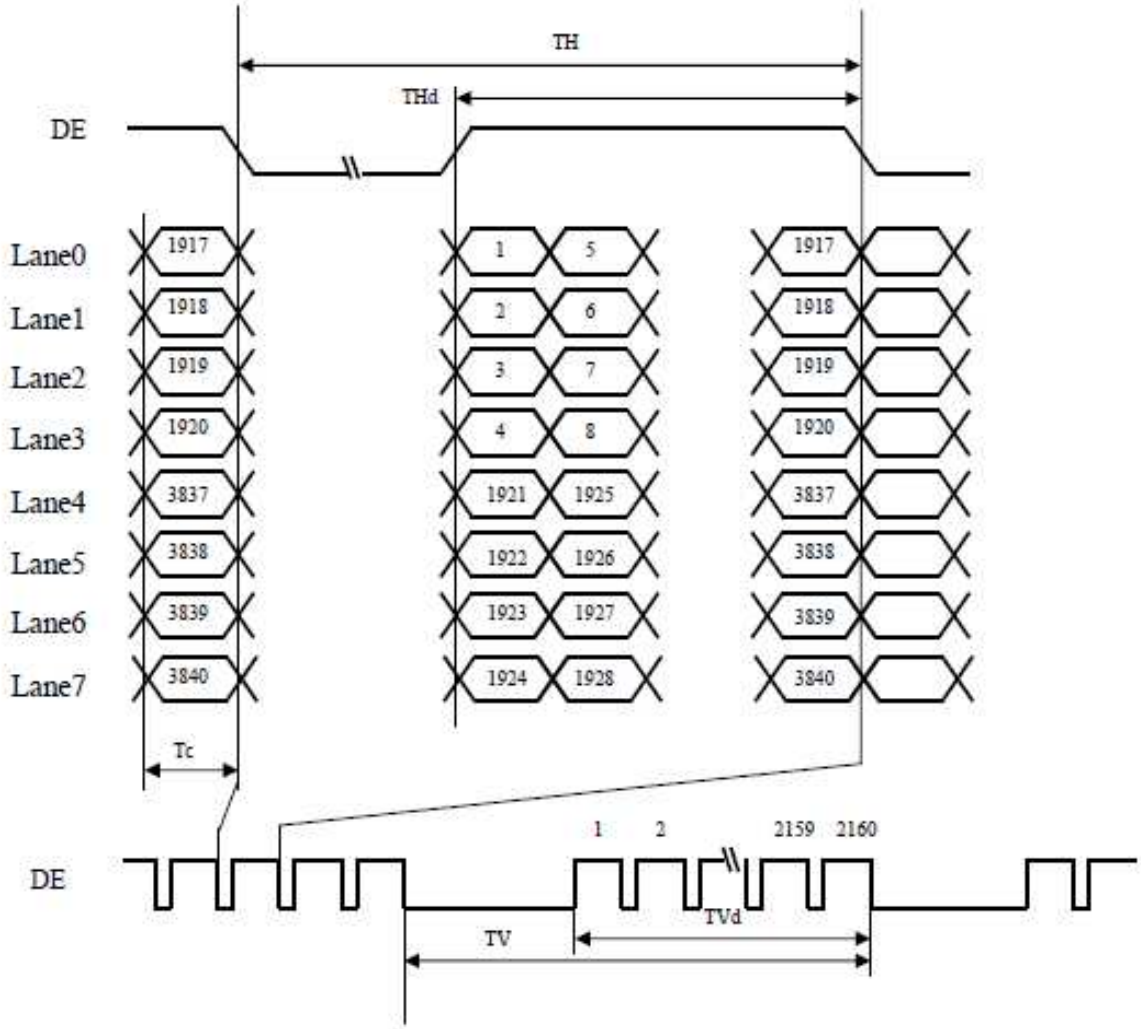


Fig.6 Timing diagram of input signals

4.6. Input Data Signal, Basic Color and Gray Scale of Each Color (with C-PWB "JE0DZ1C0435")

Colors & Gray Scale			Data signal																														
			R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	---																														
	---	---																														
	---	GS1021	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1022	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	---																														
	---	---																														
	---	GS1021	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	---	GS1022	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green	GS1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	---	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	---	---																														
	---	---																														
	---	GS1021	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
	---	GS1022	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Blue	GS1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

- 0: Low level voltage / 1: High level voltage
- Each basic color can be displayed in 1021-gray-scale from 10-bit data signals. According to the combination of total 30-bit data signals, about 1-billion-color display can be achieved on the screen.

5. Optical Characteristics (with C-PWB "JE0DZ1C0435")

Ta = 25 °C, 60 Hz Typical Timing Input to the C-PWB

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range [1]	Horizontal	θ 21 θ 22	CR ≧ 10	70	88	-	deg.	
	Vertical	θ 11 θ 12		70	88	-	deg.	
Contrast ratio [2]		CRn	θ = 0 deg.	-	4000	-	-	
Response time [3]		τ_{rd}		-	8	-	ms	Topa=30 °C
Chromaticity	White	Wx		Typ-0.03	0.281	Typ+0.03	-	
		Wy		Typ-0.03	0.288	Typ+0.03	-	
	Red	Rx		Typ-0.03	0.642	Typ+0.03	-	
		Ry		Typ-0.03	0.332	Typ+0.03	-	
	Green	Gx		Typ-0.03	0.299	Typ+0.03	-	
		Gy		Typ-0.03	0.601	Typ+0.03	-	
	Blue	Bx		Typ-0.03	0.151	Typ+0.03	-	
		By		Typ-0.03	0.064	Typ+0.03	-	
Transmittance [4]	White	Tr		-	5.1	-	%	

- Using the C-PWB "JE0DZ1C0435" and the SDP Standard LED Backlight System.
- Measuring after a backlight luminance is stable.
- Gamma Correction, Color-Gradation Correction, and Over-Shoot Driving are valid with the C-PWB "JE0DZ1C0435".
- Measurement equipment is the following,
- Design the backlight in such a way that luminance via TFT-LCD-panel become under 420 cd/m^2 at a maximum. In case the actual luminance condition is higher than above, separate agreement has to be defined based on the evaluation result that both party agreed.

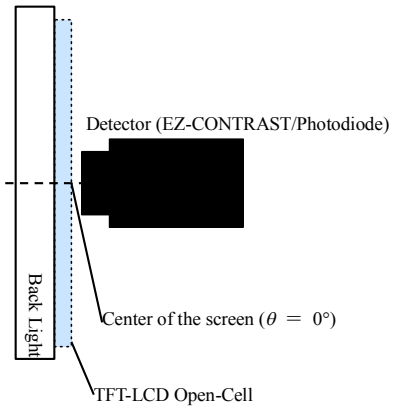


Fig.7-1 Measurement of viewing angle range and Response time.
Viewing angle range: EZ-CONTRAS
Response time: Photodiode

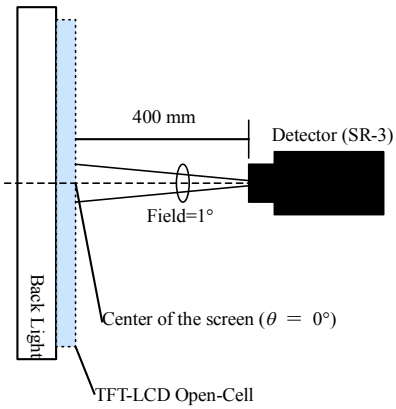


Fig.7-2 Measurement of Contrast, Luminance, Chromaticity.

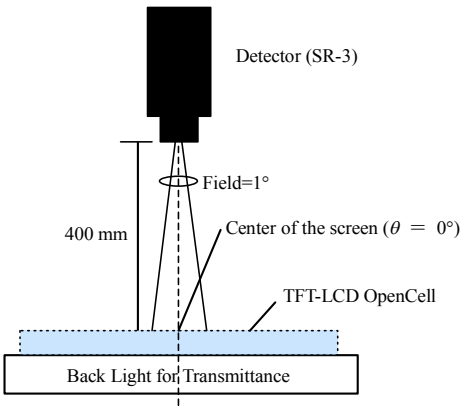


Fig.7-3 Measurement method of panel transmittance

Fig.7 Optical measuring equipment

1) The viewing angle range is defined as the following,

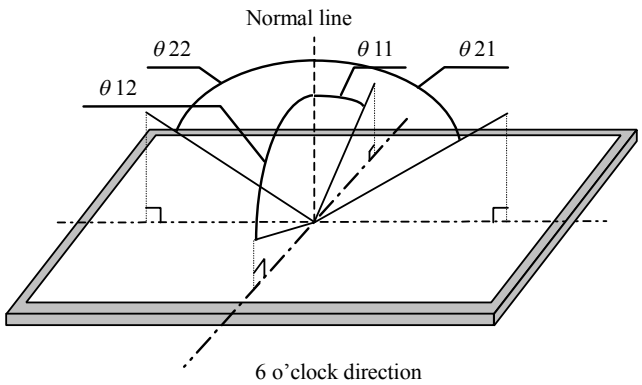


Fig.9 Measurement method of panel transmittance

2) The contrast ratio is defined as the following,

$$\text{Contrast Ratio} = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

3) The response time is defined as the following,

$$\tau_{rd} = \{\sum(\tau_r : x-y) + \sum(\tau_d : x-y)\}/20$$

τ_{rd} is an average value of a switching time from five luminance levels (0%, 25%, 50%, 75%, and 90%) to five luminance levels (0%, 25%, 50%, 75%, and 90%).

*****The following luminance level of 90% specification defines TV-signal (100IRE) level.

		Luminance level of End (y)				
		0%	25%	50%	75%	90%
Luminance level of Start (x)	0%		τ_r: 0%-25%	τ_r: 0%-50%	τ_r: 0%-75%	τ_r: 0%-90%
	25%	τ_d: 25%-0%		τ_r: 25%-50%	τ_r: 25%-75%	τ_r: 25%-90%
	50%	τ_d: 50%-0%	τ_d: 50%-25%		τ_r: 50%-75%	τ_r: 50%-90%
	75%	τ_d: 75%-0%	τ_d: 75%-25%	τ_d: 75%-50%		τ_r: 75%-90%
	90%	τ_d: 90%-0%	τ_d: 90%-25%	τ_d: 90%-50%	τ_d: 90%-75%	

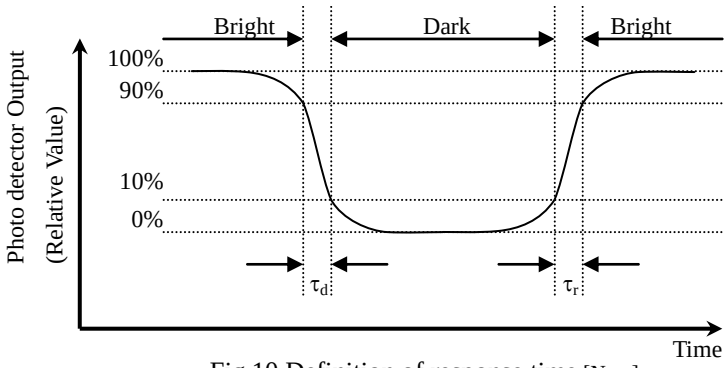


Fig.10 Definition of response time [Note]

[Note]τ_d and τ_r are defined the arrival time from 10% to 90%.

・The average value of before switching :0%

・The average value of after switching :100%

4) The transmittance is defined as the following,

$$\text{Transmittance} = \frac{\text{OpenCell luminance with all pixels white and backlight lighting}}{\text{Backlight luminance}}$$

6. Shipping Specifications

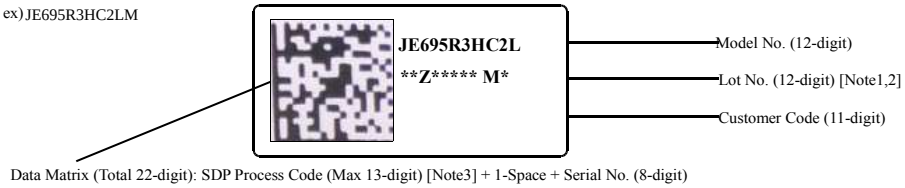
6.1.Packing Form

	1-palette	1-box
Size	1855 x 1144 x 975(H) [mm]	176(H) [mm]
Q'ty	132 Open-Cells (6 boxes)	22 Open-Cells
Mass	About 700 kg	About 115 kg

- Refer to the attached drawing for details. (Page 20)
- This packing unit is not guaranteed other than shipment by the palette.

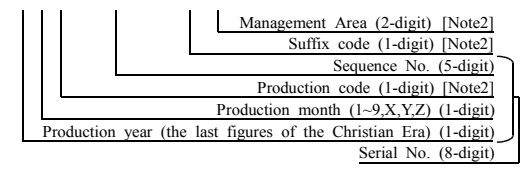
6.2. Label

a) Open-Cell Serial Label



This label is pasted on the S-PWB. Please refer to the Open Cell Outline for the pasting area.(P19)

[Note1] How to express Lot No.



[Note2] Production Code & Suffix Code & Customer Code

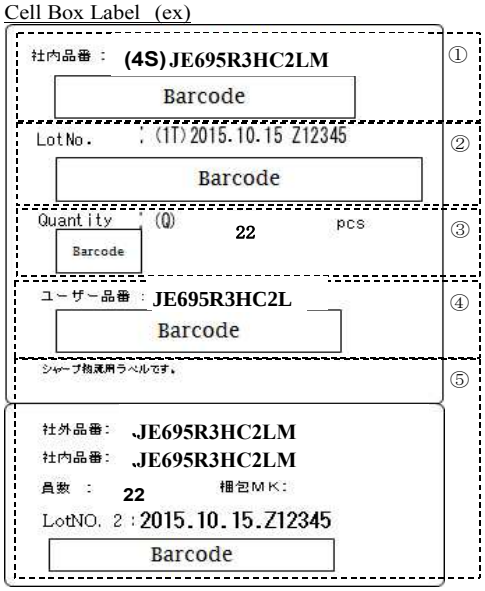
Plant	Model No.	Production Code	Suffix Code	Management area (internal code)	Customer Code	Note
Sakai	JE695R3HC2L	Z	M	(1-alphabet)	-	

[Note3] SDP Process Code (Max.13-digit)
ex) JE695R3HC2L+suffix code+space

b) Packing Labels

These labels are pasted on a cell box and the packing carton.

Cell Box Label (ex)



Packing Label (ex)

[Note1] This code may differ from "Model No. & Suffix".

1 Model No. & Suffix Code
2 Lot No. (Date)
3 Quantity
4 Customer's Code:
5 SHARP(SDP) Logistics Management Area

1 SHARP(SDP) Logistics Management Area
2 Model No & Suffix code
3 Lot No. (Date)
4 Quantity
5 Customer's Code:
6 SHARP(SDP) Logistics Management Area

7. Reliability Test

No.	Test item (Test sample form)	Condition
1	High temperature storage test (Open-Cell with C-PWB)	Ta = 60 ºC, 240 hours
2	Low temperature storage test (Open-Cell with C-PWB)	Ta = -25 ºC, 240 hours
3	High temperature and high humidity operation test (Open-Cell with C-PWB)	Ta = 40 ºC, 95% RH, 240 hours (No condensation)
4	High temperature operation test (Open-Cell with C-PWB)	Ta = 50 ºC, 240 hours *Panel surface temperature 60 ºC
5	Low temperature operation test (Open-Cell with C-PWB)	Ta = 0 ºC, 240 hours
6	Vibration test (1 Cell Box with full Open-Cells)	X and Y direction: 15 min, Z direction: 60 min. 5 Hz to 50 Hz acceleration velocity: 1.0 G, Sweeping ratio: 3 min
7	Drop test (1 Cell Box with full Open-Cells)	Height: 15 cm (1 face and 2 sides) Number: 3 times (1 time in each of drop direction)

- Result evaluation criteria:
  Under the display quality test condition with normal operation state, there shall be no change, which may affect practical display function.

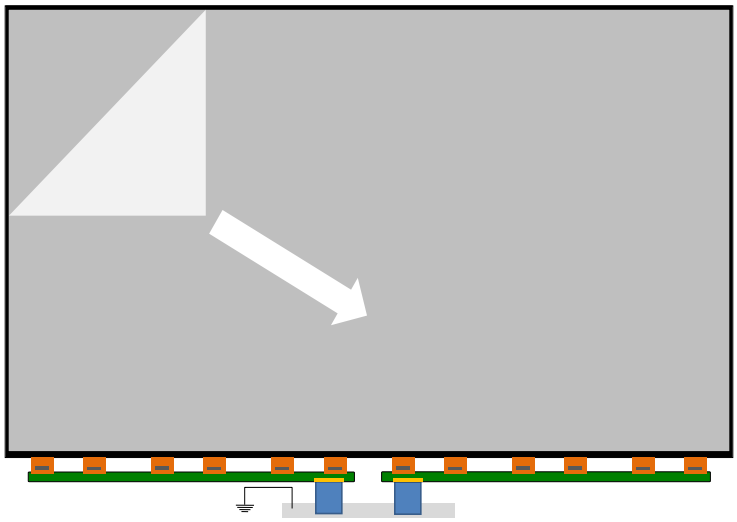
8. Precautions

a) Since this Open-Cell consists of TFTs and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharges, persons who are handling the Open-Cell should be grounded through adequate methods such as the anti-static wrist band. Connector pins should not be touched directly with bare hands.

- Reference : Process control standard of SDP

	Item	Management standard value and performance standard
1	Anti-static mat (shelf)	1 to 50 [Mohm]
2	Anti-static mat (floor, desk)	1 to 100 [Mohm]
3	Ionizer	Attenuate from ±1000 V to ±100 V within 2 sec
4	Anti-static wrist band	0.8 to 10 [Mohm]
5	Anti-static wrist band entry and ground resistance	Less than 1000 ohm
6	Temperature	22 to 26 [ºC]
7	Humidity	60 to 70 [%]

b) This Open-Cell is with the Protection Film on Polarizers. Please take care following notices within the removal of protection films.



- Be sure to peel off slowly (recommended more than 18 sec) and constant speed.
- Peeling direction shows Fig.
- Be sure to ground person with adequate methods such as the anti-static wrist band.
- Be sure to ground all terminals of the S-PWB while peeling of the protection film.
- Ionized air should be blown over during peeling action.
- The protection film must not touch drivers and S-PWBs.
- If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.

Fig.11 Direction of peeling off a protection film

c) Since the polarizer is easily damaged, pay attention not to scratch it.
d) When the polarizer is soiled, wipe it with the absorbent cotton or other soft cloth.
e) Since this TFT-LCD-panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.
f) When this TFT-LCD-panel surface gets strong pressures locally by being hit or pressed strongly by something, display Mura might remain permanently at the area where such pressures are applied. Do not push or hit by the power beyond 10N for active area of display.
g) For GOA circuit part, do not push or hit the power beyond 2.5kg/cm^2 and avoid continuous force more than 30 seconds.

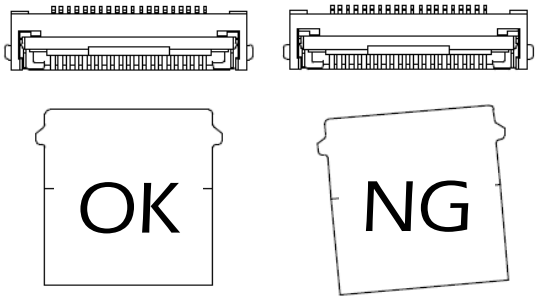
h) Since the TFT is shifted a threshold with photo excitation, shade the outside of the back polarizer from the backlight.
i) There is a common electrode with the CF Glass Edge of this TFT-LCD Panel. Do not touch the CF Glass Cut Line with conductive materials since an abnormal display may occur.
j) Please don't warp or twist the TFT-LCD-panel at handling and be sure to use suction jig at handling of the Open-Cell to prevent any external damage including warpage, cosmetic dirt and scratch.

Note: This limit is only for a short time at handling of the TFT-LCD-panel.
The module and cabinets need to be designed not to add extra stress to the TFT-LCD-panel that cause warp or twist.

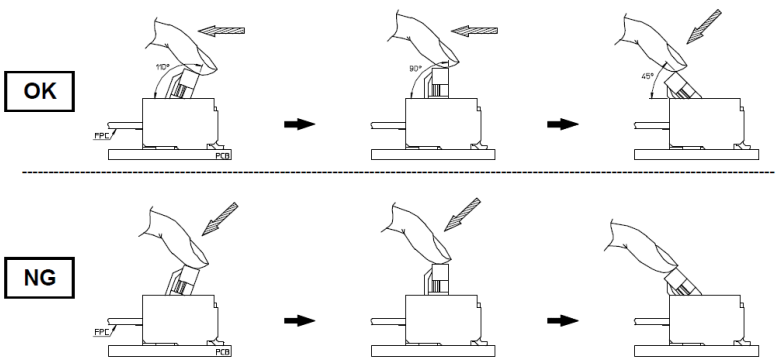
Fig.12 Limit of warpage at handling of panel

k) This Open-Cell has some PWBs, take care to keep them from any stress or pressure when handling or installing the Open-Cell, otherwise some of electronic parts on the PWB may be damaged.
l) To prevent the disconnection of S-SOFs by the thermal shock or physical damage, design the module not to fix S-PWBs with screws or tape.
m) When handling the Open-Cell and assembling them into cabinets, be noted that a long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the Open-Cell.
n) Applying too much force and stress to PWBs and SOFs may cause a malfunction electrically and mechanically.
o) In case that the SOF is needed to bend, note that the radius of bending have to be over 0.65 mm in 2 mm outside from the Driver-IC edge.
p) To radiate a heat of Source-Driver-IC(S-IC) s, the recommended operating maximum temperature is 125 ºC at a chip surface, design the module to contact the opposite side of S-ICs with a high thermal conductivity material.[Fig.13-1]
q) Handle with care based on the general connector's specification when inserting and removing FFCs or FPCs.
r) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.
s) Turn off the power supply when inserting or disconnecting the cable.
t) This Open-Cell has high frequency circuits. Sufficient suppression to EMI should be done by system manufacturers.
u) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.
v) Since long contact with water may cause discolorations or spots, wipe off water drop immediately.
w) The chemical compound, which causes the destruction of ozone layer, is not being used.
x) Instruction of connector upon usage.

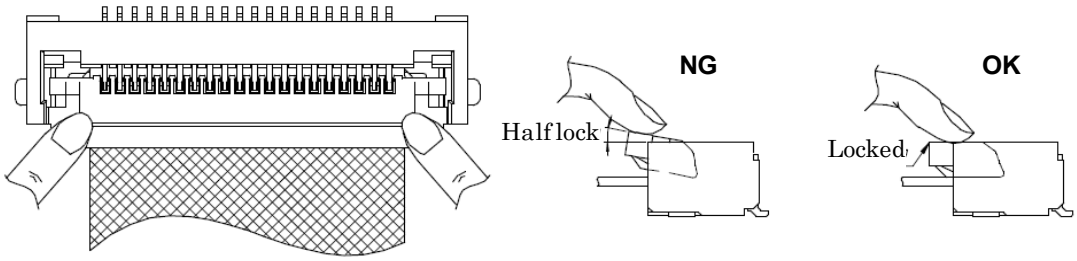
a) Do with the actuator opened completely, and insert it in the interior of the insertion entrance surely Horizontally When you insert FFC or FPC. (Please put the FFC or FPC tab in the ditch of the housing surely with the FFC or FPC tab.) Might it become short defective, and it causes the corner to transform the caught terminal into the terminal by the pitch gap when inserting it right and left and diagonally.



b) Please add force in the direction where the actuator is held and do by rotating it pushing in parallel to the C-PWB direction when becoming 90°or less as shown in the figure below until the angle of the actuator becomes 90°or less when you shut the actuator. Please do not add the force to rotary axis of actuator in the direction that the actuator is off.



c) About the lock operation
When you lock, it should be push on both sides of the actuator. And it is necessary to confirm that the actuator is surely shut.



y) This Open-Cell is corresponded to RoHS. "R.C." label on the side of a palette shows it.
z) When any question or issue occurs, it shall be solved by mutual discussion.
aa) Be sure to design the LCD module and cabinet not to bend the S-SOF and G-SOF at the unbendable area [Fig. 13-2] to avoid the disconnection of wires or removal of IC chip from film.
bb) In case that S-SOF and G-SOF are needed to bend, please note that the radius of bending have to be over 0.65 mm [Fig. 13-2].

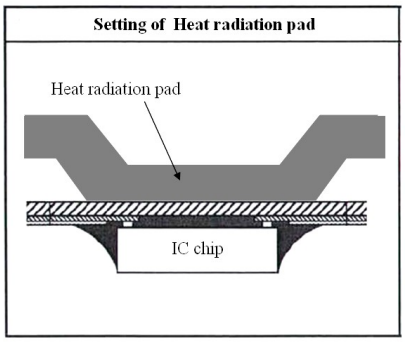


Fig.13-1 Diagram of setting example of heat radiation pad on S-SOF

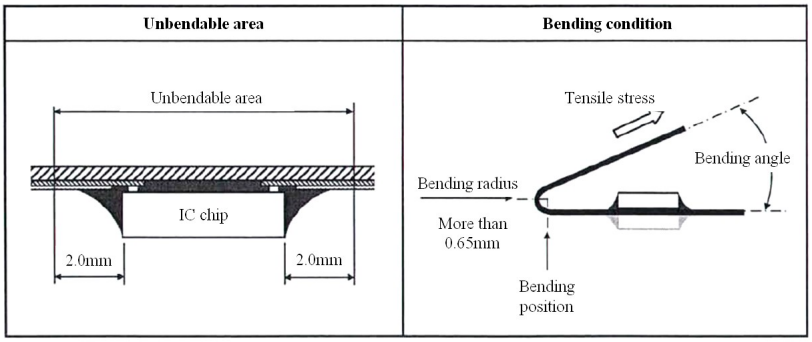
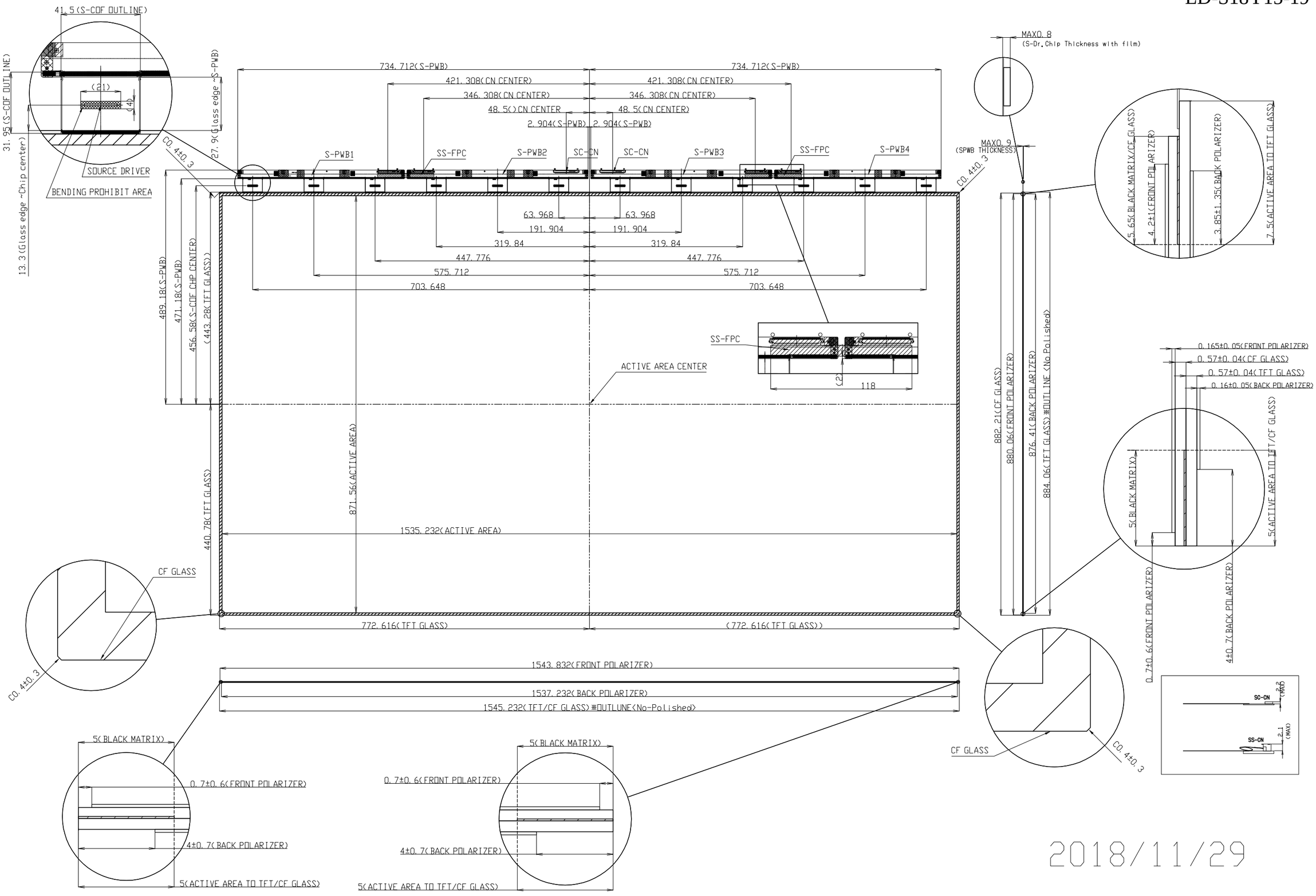


Fig.13-2 Unbendable area and Bending condition of S-SOF/G-SOF

cc) Be sure to design the LCD module and cabinet not to fix with SPWB by screws to prevent the disconnection of S-SOF by the thermal shock or physical damage.
dd) When the panel surface gets the strong pressure locally by being hit or pressed strongly by something, display Mura might remain permanently at the area where such pressure is applied. Therefore, please be careful well of handling panel in your production process and also call end customer attention for careful handling.
ee) Since damage may be done from the sticker within permission, please do not use the corner edge of a panel for positioning use or holding a panel.

9. Storage Conditions of Open-Cell in Cell-Box

Temperature	0°C to 40°C
Humidity	95% RH or less
Reference condition	20°C to 35°C, 85% RH or less (summer) 5°C to 15°C, 85% RH or less (winter) The total storage time(40°C, 95% RH) :240 hours or less
Sunlight	Shelter a production from the direct sunlight.
Atmosphere	Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
Notes	Put the box on a palette or a base, do not put it on a floor, and store them with removing from a wall. Take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment.
Storage life	1 year



2018/11/29

Fig.14 JE695R3HC2L Open cell outline

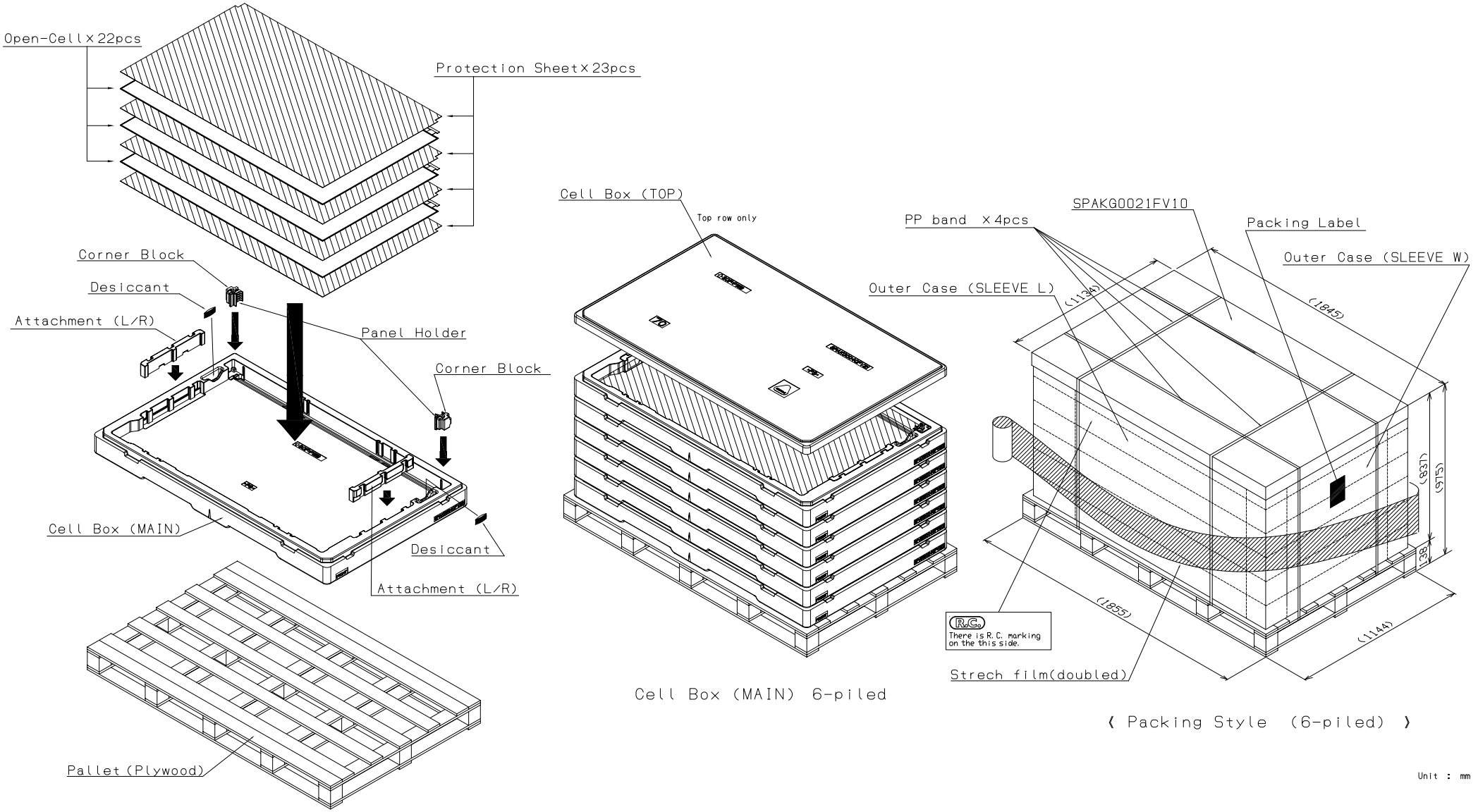


Fig.15 Packing form of JE695R3HC2L