PREPARED BY: DATE	Sakai SIO International Guangzhou CO.,LTD	SPEC No:C20046B
		FILE No:
APPROVED BY: DATE		ISSUE: 2021.01.28
		PAGE: 28 pages

CORPORATE RESEARCH AND DEVELOPMENT GROUP

SPECIFICATION

MODEL No. JR645R3HB1K

DEVICE SPECIFICATION

FOR
TFT-LCD Open Cell

CUSTOMER'S APPROVAL

DATE

BY

Title&Department

Company

Approved By	Prepared By
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超视堺国际科技（广州）有限公司

RECORDS OF REVISION

Model: JR645R3HB1K

SPEC No.	DATE	REVISED No.	SUMMARY PAGE	SUMMARY	NOTE
C20046B	Jan. 28. 2021		All	The Approval Specification was been released.	

1. Application

This specification applies to the color TFT-LCD Open-Cell “JR645R3HB1K”.

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2. Overview

This Open Cell (JR645R3HB1K) is a color active matrix LCD Open Cell incorporating amorphous silicon TFT (Thin Film Transistor), Polarizers, Source-PWBs, Source-Drivers. The following content can be achieved in using C-PWB (RUNTK0018HVxx) that SDP specifies. Graphics and texts can be displayed on a 3840 x RGB x 2160 dots panel with one billion colors by using USIT to interface,+12.0V of DC supply voltages.

This Open Cell is designed for the Single Frame Rate driving. It can be displayed the moving picture smoothly to apply the Over Shoot driving (O/S driving) technology for the control circuit. In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.
With combination of these technologies, motion blur can be reduced and clearer display performance can be realized.
[Caution] You should design thermal conductive interface pad and C-PWB cover enough to radiate heat from IC in Source-Drivers and mounted parts on C-PWB.

This Open-Cell has below features.

- 4K2K (3840 x RGB x 2160) High Resolution
- VNB (Very Narrow Bezel) amorphous-silicon-TFT-LCD-Panel
- UV2A High Contrast and Transmittance Pixel Aperture
- Gate on array (GOA) structure
- Wide-View angle with MPD (Multi-Pixel-Driving)
  USIT Driver Interface Technology for V-by-One® HS control system with the Special C-PWB “RUNTK0018HVxx”

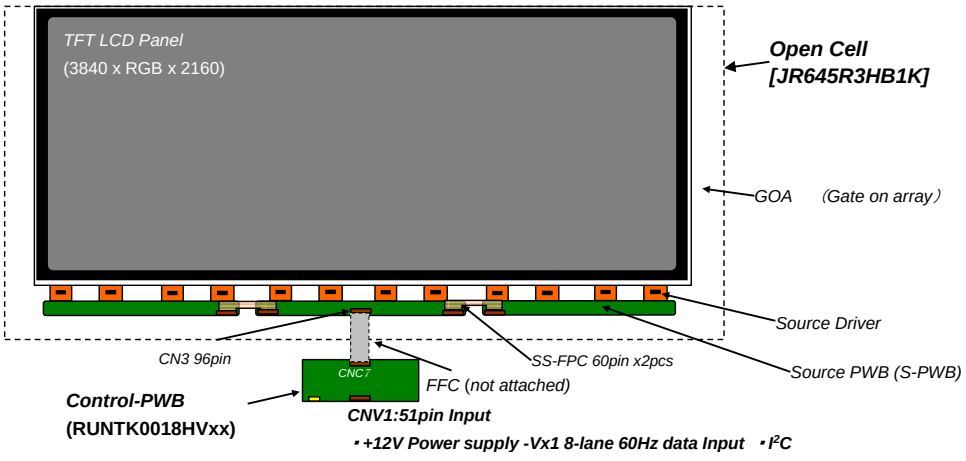


Fig.1 Diagram of the Open Cell and CPWB

3. Mechanical Specifications

Parameter	Specification	Unit
Display size (Active Area)	1428.48 (H) x 803.52 (V) 1638.96(Diagonal) [64.5”]	mm mm
Pixel format	3840 (H) x 2160 (V) (1pixel = R + G + B dot)	pixel
Pixel pitch	0.372(H) x 0.372 (V)	mm
Pixel configuration	B,G,R vertical stripe	-
Display mode	Normally black	-
Outline dimensions [1)]	1438.48 (H) x 858.66 (V) x 3.6 (D)	mm
Mass	3.42±5%	kg
Surface treatment [2)]	- Front polarizer: Low-Haze(less than 5%) Anti-Glare, Hard-Coating(2H and more) - Rear polarizer: Hard-Coating less	-

1) The thickest point is the CN on the S-PWB, the display area thickness is shown the outline drawing in the last Page.
2) With the protection film removed.

4. Interface Specifications

4.1. Input Interface Specifications

CNV1 of C-PWB “ RUNTK0018HVxx”: Vx1 8-Lane Data

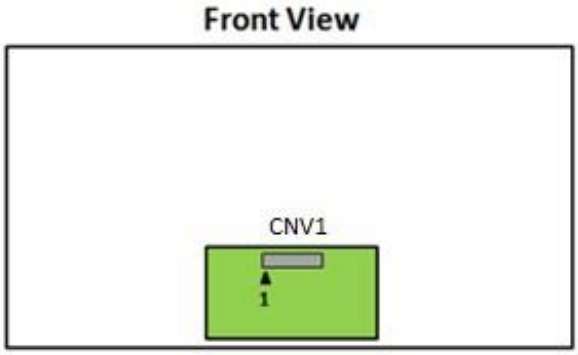
- Using Connector : 0-5112215-5 (XDYT), F05035-51P-A（CT）
- Recommend Mating FFC drawing [3)]
- Mating V-by-One® HS Transmitter : THCV215 (THine) or Equivalent Device

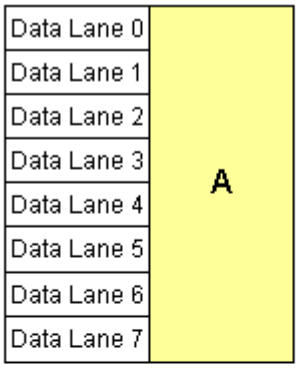
Pin No.	CNV1 of C-PWB RUNTK0018HVxx		
	Pin Name	Signal	Remark
1	VCC	Power Supply	+12.0V[5)]
2	VCC	Power Supply	+12.0V[5)]
3	VCC	Power Supply	+12.0V[5)]
4	VCC	Power Supply	+12.0V[5)]
5	VCC	Power Supply	+12.0V[5)]
6	VCC	Power Supply	+12.0V[5)]
7	VCC	Power Supply	+12.0V[5)]
8	VCC	Power Supply	+12.0V[5)]
9	NC	NC (OPEN)	[4)]
10	GND	GND	
11	GND	GND	
12	GND	GND	
13	GND	GND	
14	GND	GND	
15	NC	-	[4)]
16	NC	-	[4)]
17	NC	-	[4)]
18	NC	-	[4)]
19	NC	-	[4)]
20	NC	-	[4)]
21	NC	-	[4)]
22	NC	-	[4)]
23	AGE	Aging pin	L: Aging function off H : Aging function on(3.3 V) [7)]
24	NC	-	[4)]
25	HTPDN	Hot Plug Detect Output	Normally Low[6)]
26	LOCKN	Lock Detect Output	L : Lock / Hi-Z : Unlock (Open Drain) [2)]
27	CML GND	GND	
28	Rx0n	Vx1 Input Data_Lane-0	[1)]
29	Rx0p	Vx1 Input Data_Lane-0	[1)]
30	CML GND	GND	
31	Rx1n	Vx1 Input Data_Lane-1	[1)]
32	Rx1p	Vx1 Input Data_Lane-1	[1)]
33	CML GND	GND	
34	Rx2n	Vx1 Input Data_Lane-2	[1)]
35	Rx2p	Vx1 Input Data_Lane-2	[1)]
36	CML GND	GND	
37	Rx3n	Vx1 Input Data_Lane-3	[1)]
38	Rx3p	Vx1 Input Data_Lane-3	[1)]

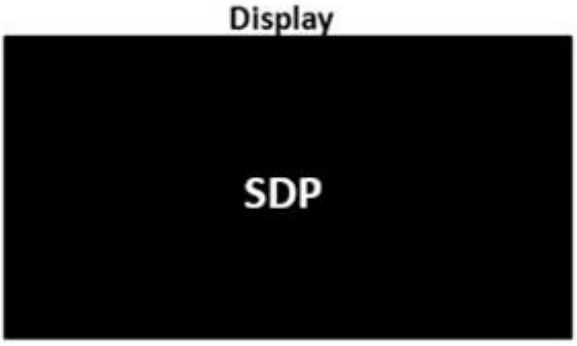
39	CML GND	GND	
40	Rx4n	Vx1 Input Data_Lane-4	1)
41	Rx4p	Vx1 Input Data_Lane-4	1)
42	CML GND	GND	
43	Rx5n	Vx1 Input Data_Lane-5	1)
44	Rx5p	Vx1 Input Data_Lane-5	1)
45	CML GND	GND	
46	Rx6n	Vx1 Input Data_Lane-6	1)
47	Rx6p	Vx1 Input Data_Lane-6	1)
48	CML GND	GND	
49	Rx7n	Vx1 Input Data_Lane-7	1)
50	Rx7p	Vx1 Input Data_Lane-7	1)
51	CML GND	GND	
Pin No.	Pin Name	Signal	Remark
	CNV1 of C-PWB	RUNTK0018HVxx	

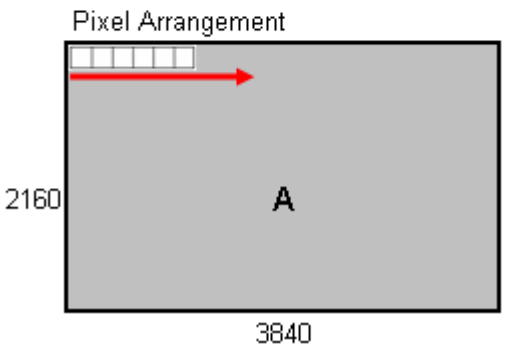
Note (1) V-by-One HS Data Mapping

Area	Lane	Data Stream
A	Lane 0	1, 9, 17, ..., 3825, 3833
	Lane 1	2, 10, 18, ..., 3826, 3834
	Lane 2	3, 11, 19, ..., 3827, 3835
	Lane 3	4, 12, 20, ..., 3828, 3836
	Lane 4	5, 13, 21, ...,3829, 3837
	Lane 5	6, 14, 22, ..., 3830, 3838
	Lane 6	7, 15, 23, ..., 3831, 3839
	Lane7	8, 16, 24, ..., 3832, 3840

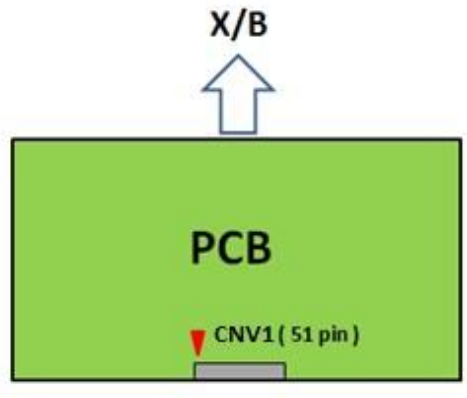




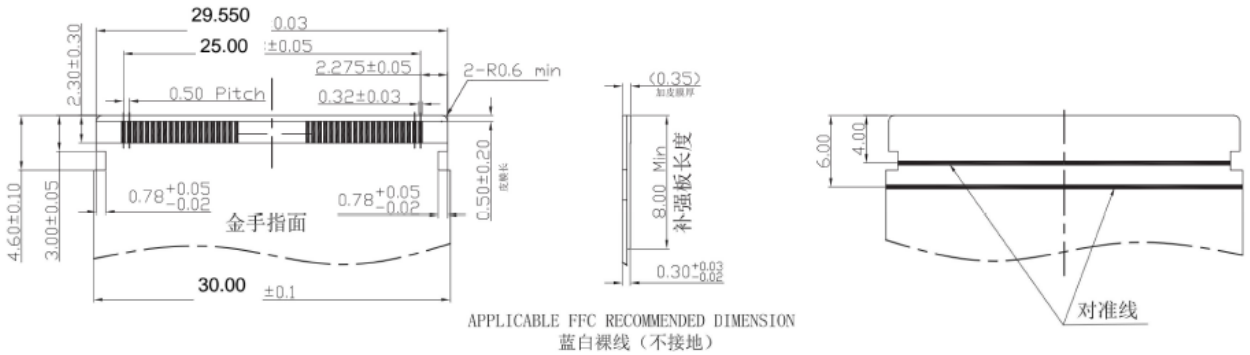




Note (2) V-by-One HS connector pin order defined as follows



Note (3) V-by-One connector Recommend Mating FFC drawing as below

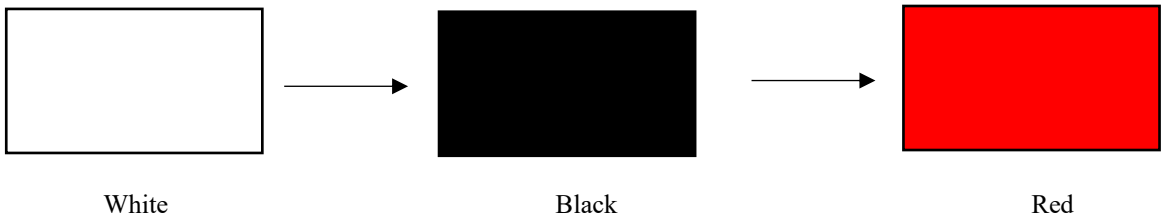


Note (4) Reserved for internal use. Please leave it open.

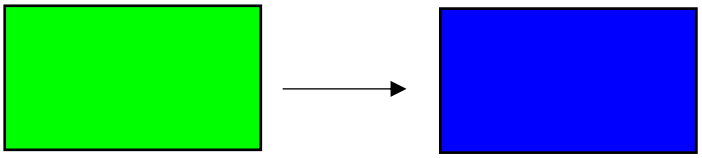
Note (5) Power input (+12V), please check the current rating of FFC cable to meet the power consumption requirement.

Note (6) This pin connect to ground internal, but it could be open.

Note (7) Connect to the GND or NC. If connected to high level (3.3V), it will enter the aging mode. Aging pattern have White → Black → Red → Green → Blue.



White Black Red

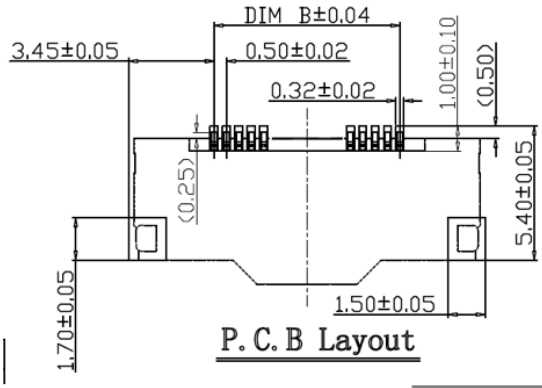


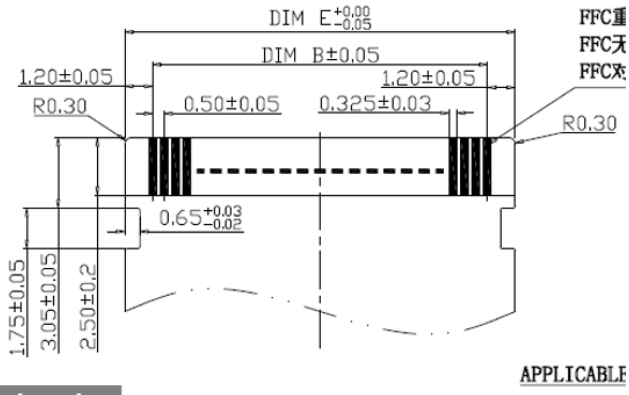
Green Blue

4.2. Connection between C-PWB“RUNTK0018HVxx” and S-PWB

CNC7 (Output signals)

- C-PWB Output Connector (CNC7) : 9-05582101-6 (XDYT) ， F05058-96P-W（CT）
- Recommended Terminal Figure of FFC or FPC :





DIM B （mm）	DIM E （mm）
47.5	49.9

[Note] Contact SDP or the connector manufacturer for details of the FFC or FPC design

Output：CNC7 of C-PWB “RUNTK0018HVxx”			Input：Connector of S-PWB		
Pin No.	**Pin Name**	**Description**	**Pin No.**	**Pin Name**	**Description**
1	NC	NC	96	NC	NC
2	GND	GND	95	GND	GND
3	NC	NC	94	NC	NC
4	NC	NC	93	NC	NC
5	VCM	TFT-LCD-Panel Common Voltage	92	VCM	TFT-LCD-Panel Common Voltage
6	VCM	TFT-LCD-Panel Common Voltage	91	VCM	TFT-LCD-Panel Common Voltage
7	NC	NC	90	NC	NC
8	NC	NC	89	NC	NC
9	NC	NC	88	NC	NC
10	GEP	Gate End Pulse	87	GEP	Gate End Pulse
11	GSP	Gate Start Pulse	86	GSP	Gate Start Pulse
12	CK4	Gate Clock 4	85	CK4	Gate Clock 4
13	CK5	Gate Clock 5	84	CK5	Gate Clock 5
14	CK6	Gate Clock 6	83	CK6	Gate Clock 6
15	CK7	Gate Clock 7	82	CK7	Gate Clock 7
16	CK8	Gate Clock 8	81	CK8	Gate Clock 8
17	CK1	Gate Clock 1	80	CK1	Gate Clock 1
18	CK2	Gate Clock 2	79	CK2	Gate Clock 2
19	CK3	Gate Clock 3	78	CK3	Gate Clock 3
20	NC	NC	77	NC	NC
21	NC	NC	76	NC	NC
22	NC	NC	75	NC	NC
23	NC	NC	74	NC	NC
24	NC	NC	73	NC	NC
25	NC	NC	72	NC	NC
26	VGL_AA	Gate Low Power Supply	71	VGL_AA	Gate Low Power Supply
27	VGL_AA	Gate Low Power Supply	70	VGL_AA	Gate Low Power Supply
28	NC	NC	69	NC	NC
29	NC	NC	68	NC	NC
30	Panel_3.3V	SPI FLASH Power Supply	67	Panel_3.3V	SPI FLASH Power Supply
31	IO2 (WP)	SPI FLASH WP	66	IO2 (WP)	SPI FLASH WP
32	IO1 (DO)	SPI FLASH DO	65	IO1 (DO)	SPI FLASH DO
33	IO0 (DI)	SPI FLASH DI	64	IO0 (DI)	SPI FLASH DI
34	CS	SPI FLASH CS	63	CS	SPI FLASH CS
35	SCK	SPI FLASH CLK	62	SCK	SPI FLASH CLK
36	IO3 (HOLD)	SPI FLASH HOLD	61	IO3 (HOLD)	SPI FLASH HOLD
37	V1D8D	S-IC_VCC	60	V1D8D	S-IC_VCC
38	V1D8D	S-IC_VCC	59	V1D8D	S-IC_VCC
39	V1D8D	S-IC_VCC	58	V1D8D	S-IC_VCC
40	V1D8D	S-IC_VCC	57	V1D8D	S-IC_VCC
41	OTP	SEL_EQ_ID	56	OTP	SEL_EQ_ID
42	SBC	USIT-SBC	55	SBC	USIT-SBC
43	GND	GND	54	GND	GND
44	L1P	Differential Data and Signal(L1P)	53	L1P	Differential Data and Signal(L1P)
45	L1N	Differential Data and Signal(L1N)	52	L1N	Differential Data and Signal(L1N)

46	GND	GND	51	GND	GND
47	L2P	Differential Data and Signal(L2P)	50	L2P	Differential Data and Signal(L2P)
48	L2N	Differential Data and Signal(L2N)	49	L2N	Differential Data and Signal(L2N)
49	GND	GND	48	GND	GND
50	L3P	Differential Data and Signal(L3P)	47	L3P	Differential Data and Signal(L3P)
51	L3N	Differential Data and Signal(L3N)	46	L3N	Differential Data and Signal(L3N)
52	GND	GND	45	GND	GND
53	L4P	Differential Data and Signal(L4P)	44	L4P	Differential Data and Signal(L4P)
54	L4N	Differential Data and Signal(L4N)	43	L4N	Differential Data and Signal(L4N)
55	GND	GND	42	GND	GND
56	L5P	Differential Data and Signal(L5P)	41	L5P	Differential Data and Signal(L5P)
57	L5N	Differential Data and Signal(L5N)	40	L5N	Differential Data and Signal(L5N)
58	GND	GND	39	GND	GND
59	L6P	Differential Data and Signal(L6P)	38	L6P	Differential Data and Signal(L6P)
60	L6N	Differential Data and Signal(L6N)	37	L6N	Differential Data and Signal(L6N)
61	GND	GND	36	GND	GND
62	L7P	Differential Data and Signal(L7P)	35	L7P	Differential Data and Signal(L7P)
63	L7N	Differential Data and Signal(L7N)	34	L7N	Differential Data and Signal(L7N)
64	GND	GND	33	GND	GND
65	L8P	Differential Data and Signal(L8P)	32	L8P	Differential Data and Signal(L8P)
66	L8N	Differential Data and Signal(L8N)	31	L8N	Differential Data and Signal(L8N)
67	GND	GND	30	GND	GND
68	L9P	Differential Data and Signal(L9P)	29	L9P	Differential Data and Signal(L9P)
69	L9N	Differential Data and Signal(L9N)	28	L9N	Differential Data and Signal(L9N)
70	GND	GND	27	GND	GND
71	L10P	Differential Data and Signal(L10P)	26	L10P	Differential Data and Signal(L10P)
72	L10N	Differential Data and Signal(L10N)	25	L10N	Differential Data and Signal(L10N)
73	GND	GND	24	GND	GND
74	L11P	Differential Data and Signal(L11P)	23	L11P	Differential Data and Signal(L11P)
75	L11N	Differential Data and Signal(L11N)	22	L11N	Differential Data and Signal(L11N)
76	GND	GND	21	GND	GND
77	L12P	Differential Data and Signal(L12P)	20	L12P	Differential Data and Signal(L12P)
78	L12N	Differential Data and Signal(L12N)	19	L12N	Differential Data and Signal(L12N)
79	GND	GND	18	GND	GND
80	SFC	USIT-SFC	17	SFC	USIT-SFC
81	GND	GND	16	GND	GND
82	NC	NC	15	NC	NC
83	VL255	Gamma Reference Voltage	14	VL255	Gamma Reference Voltage
84	VL0	Gamma Reference Voltage	13	VL0	Gamma Reference Voltage
85	HAVDD	Source driver analog voltage	12	HAVDD	Source driver analog voltage
86	HAVDD	Source driver analog voltage	11	HAVDD	Source driver analog voltage
87	VH0	Gamma Reference Voltage	10	VH0	Gamma Reference Voltage
88	VH255	Gamma Reference Voltage	9	VH255	Gamma Reference Voltage
89	AVDD	Source Driver Power Voltage	8	AVDD	Source Driver Power Voltage
90	AVDD	Source Driver Power Voltage	7	AVDD	Source Driver Power Voltage
91	AVDD	Source Driver Power Voltage	6	AVDD	Source Driver Power Voltage
92	AVDD	Source Driver Power Voltage	5	AVDD	Source Driver Power Voltage
93	AVDD	Source Driver Power Voltage	4	AVDD	Source Driver Power Voltage
94	AVDD	Source Driver Power Voltage	3	AVDD	Source Driver Power Voltage
95	AVDD	Source Driver Power Voltage	2	AVDD	Source Driver Power Voltage
96	AVDD	Source Driver Power Voltage	1	AVDD	Source Driver Power Voltage
Pin No.	**Pin Name**	**Description**	**Pin No.**	**Pin Name**	**Description**
Output：CNC7 of C-PWB"RUNTK0018HVxx"			**Input：Connector of S-PWB**		

4.3.Absolute Maximum Ratings (with C-PWB “RUNTK0018HVxx”)

(GND = 0 V)

Parameter	Symbol	Condition	Ratings	Unit	Remark
Input Power Voltage	VCC	Ta = 25ºC	-0.3 to +13.5	V	C-PWB : VCC
Input Control Voltage	V_I	Ta = 25ºC	-0.3 to +3.6	V	C-PWB : LOCKN
Input Vx1 Data Voltage	V_{VBO}	Ta = 25ºC	-0.3 to +3.0	V	C-PWB : Rx*n/p
Storage Temperature	Tstg	-	-20 to +60	ºC	Open-Cell with C-PWB
Operation Temperature	Topa	-	0 to +50	ºC	Open-Cell with C-PWB [1)]

- Humidity 95%RH Max.(at Ta ≦ 40 ºC)
- Maximum wet-bulb temperature 39 ºC or less (at Ta > 40 ºC)
- No condensation.
- Design the module with a maintaining temperature of the panel at 60ºC or less and uniform as much as possible.
- Otherwise there is possibility to cause several issues such as “Mura” or “Gamma shift”, etc.
- Design the module with a maintaining temperature of Black Mask(BM) area of panel at 70 ºC or less and uniform as much as possible. Otherwise there is possibility to cause functional issue in GOA circuit, which is located at BM area.
  1) Refer to the C-PWB’s specification for the operation temperature of ICs on the C-PWB.
  2) The recommended operating maximum temperature of the Source-Driver-IC is 110 ºC at a chip surface.

4.4. Electrical Characteristics of Input Signals (with C-PWB “RUNTK0018HVxx”)

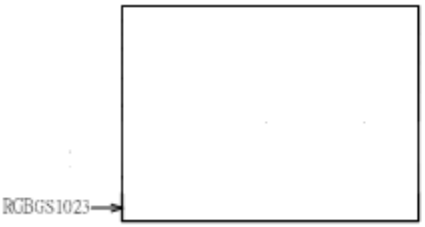
(Ta = 25 ± 2 ºC)

Item		Symbol	Min.	Typ.	Max.	Unit	Note
C-PWB Power	Supply Voltage	VCC	10.8	12	13.2	V	
	Current Dissipation [1)]	ICC	0.8		2.5	A	
	Inrush Current [2)]	Irush			4	A	
QFHD 60Hz Output Power Consumption	White Pattern	P_T	_	8.16	13.2	W	
	Horizontal Stripe	P_T	_	26.4	38.55	W	
	Black Pattern	P_T	_	8.4	12.94	W	
QFHD 60Hz Output Power Supply Current	White Pattern	-	_	0.68	1	A	
	Horizontal Stripe	-	_	2.2	2.92	A	
	Black Pattern	-	_	0.70	0.98	A	
Differential Input High Threshold		V_{RTH}	-	-	50	mV	
Differential Input Low Threshold		V_{RTL}	-50	-	-	mV	
Unit Interval		UI	250	-	617	Ps	
Differential Input Allowable Intra-pair Skew		tRISK_INTRA	-0.3	-	0.3	UI	
Differential Input Allowable Inter-pair Skew		tRISK_INTER	-5	-	5	UI	
Input Low Voltage		V_{IL}	0	-	0.7	V	
Input High Voltage		V_{IH}	2.7	-	3.6	V	
Terminal Resistor		Rt	80	100	120	Ohm	Differential Input

- In any case, input voltage should not exceed the maximum level or should not be below the minimum level including any ripple.

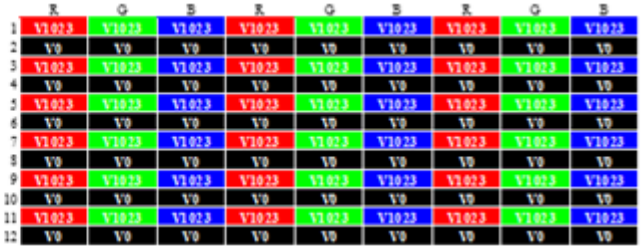
1) Definition Pattern of Current Dissipation

Typical current situation: White pattern

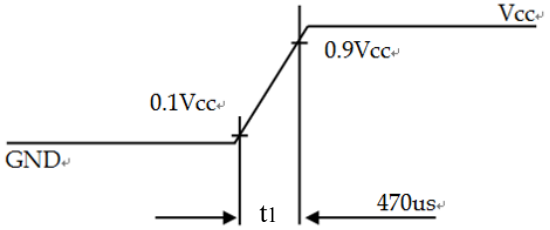


Vcc=+12.0V
CLK=74.25MHz
TH=7.4μs
TV=2250line

Max current situation: Max pattern (1-line stripe)



2) V_{CC} = +12.0V Inrush Current Waveform (Ref.t_1=470usec)



4.5. Timing Characteristics (with C-PWB " RUNTK0018HVxx")

4.5.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram. (Ta = 25 ± 2 ºC)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frequency	Data Clock	1/Tc	70	74.25	80	MHZ	(1)
V-by-One Receiver	Intra-Pair skew		-0.3	—	0.3	UI	(2)
	Inter-pair skew		-5	—	5	UI	(3)
	Spread spectrum modulation range	F_{clkin_mod}	1/Tc-0.5%	—	1/Tc+0.5%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	—	—	30	KHz	

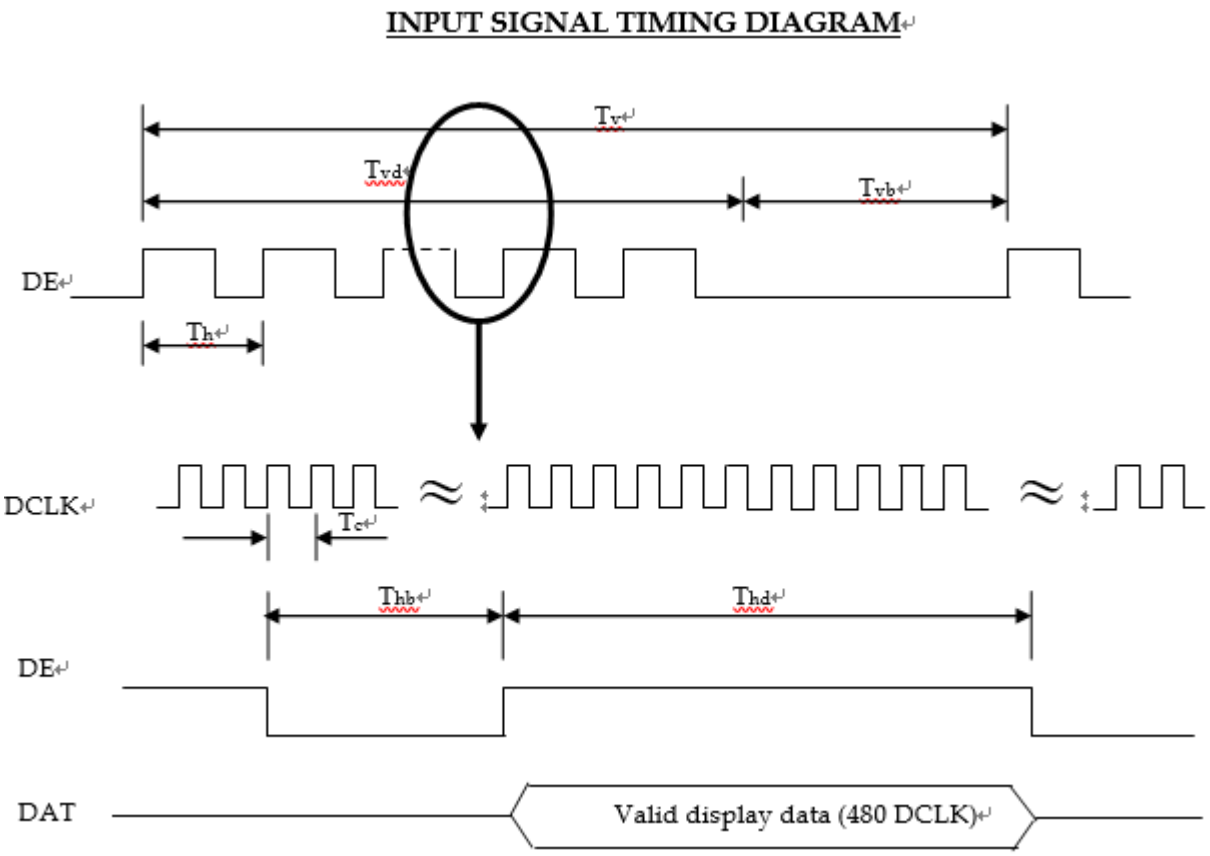
Timing spec for QFHD Frame Rate = 60Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame Rate	2D Mode		Fr	57	60	63	Hz	(5),(6)
Horizontal Frequency			Fh	122.8	135	140	KHz	
Vertical Active Display Term (8 Lane,3840X2160 Active Area)	2D Mode	Total	Tv	2240	2250	2872	Th	Tv=Tvd+Tvb
		Display	Tvd	2160				
		Blank	Tvb	80	90	712	Th	
Horizontal Active Display Term (8 Lane,3840X2160 Active Area)	2D Mode	Total	Th	530	550	702	Tc	Th=Thd+Thb
		Display	Thd	480			Tc	
		Blank	Thb	50	70	222	Tc	

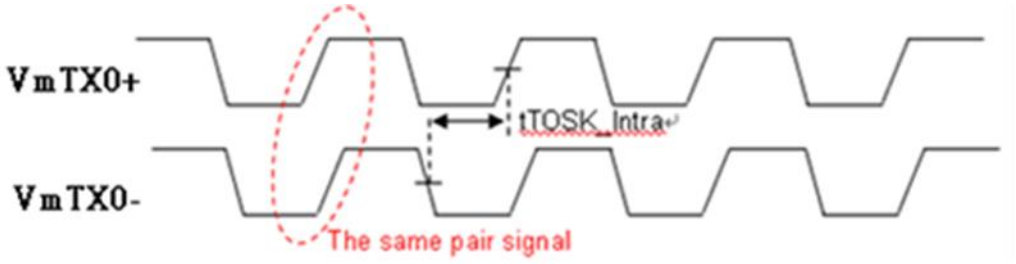
Note (1) Please make sure the range of pixel clock has follow the below equation:

Fclkin(max) ≧ Fr × Tv × Th

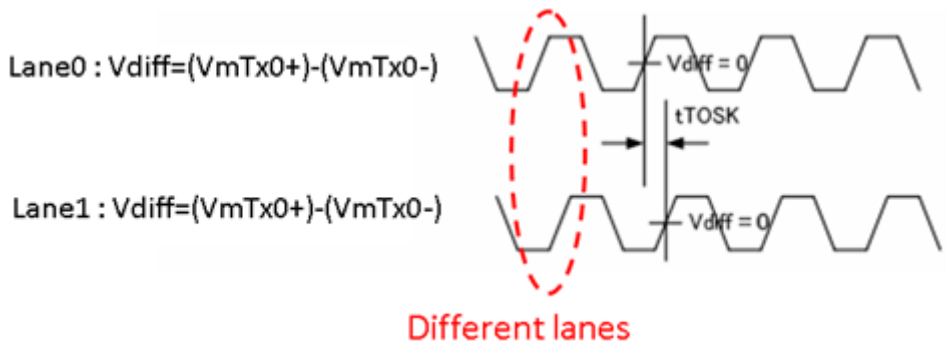
Fr × Tv × Th ≧ Fclkin(min)



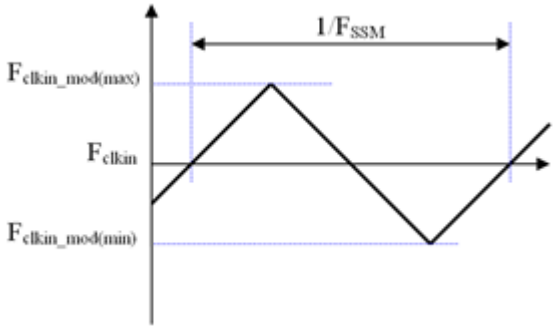
Note (2) V-by-One HS Intra-pair skew



Note (3) V-by-One HS Inter-pair skew.

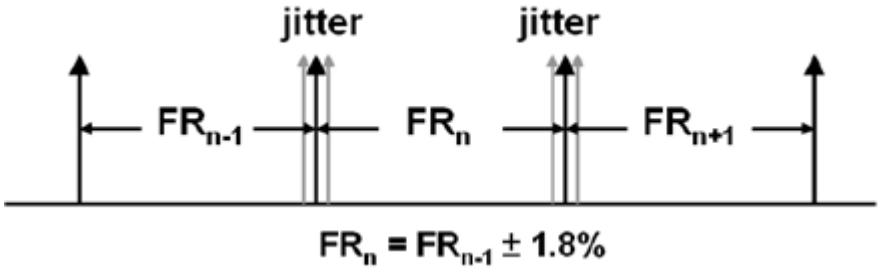


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) For converter reference signals, the frame-to-frame jitter of the input frame rate is defined as the above figures. FRn = FRn-1 ± 1.8%

Note (6) For converter reference signals, The setup of the frame rate jitter > 1.8% may result in the cosmetic LED backlight symptom.



4.5.2 Timing Diagram

4.5.2.1. V by One Input Signal Timing Diagram

The eye diagram is measured by the oscilloscope and receiver CDR characteristic must be emulated.

PLL bandwidth : 15MHz

Damping factor : 1.4

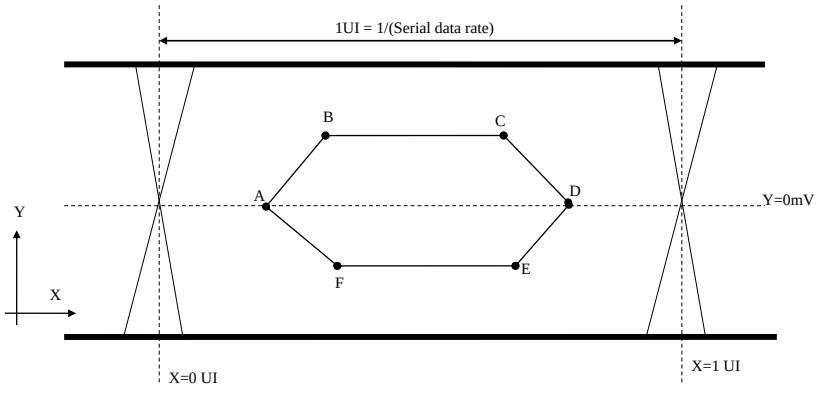


Table 1 Eye Mask Specification

	X [UI]	Y [mV]	Note
A	0.25	0	(1)
B	0.3	50	(1)
C	0.7	50	(1)
D	0.75	0	(1)
E	0.7	-50	(1)
F	0.3	-50	(1)

Note (1) Input levels of V-by-One HS signals are comes from “V-by-One HS Stander Ver.1.4”

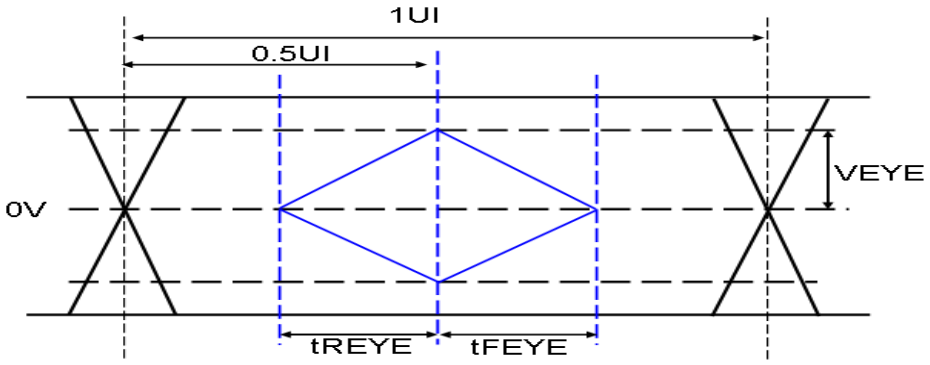
4.5.2.2. USIT Signal Timing Diagram

1. USIT AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Effective Veye Rising Time	tREYE	0.25	-	-	UI	
Effective Veye Falling Time	tFEYE	0.25	-	-	UI	
Effective Veye Level	VEYE	67.5	-	-	mV	
USIT Clock	1UI	0.333	-	0.833	ns	

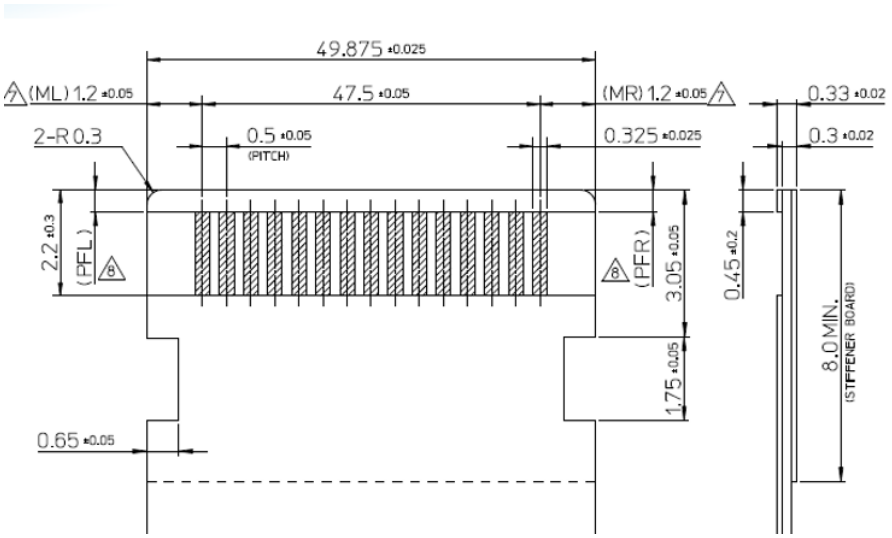
Note (1) USIT EYE diagram must be in above spec. If your application is not in our spec., SIO can not guarantee Display and function normal.

Note (2) Eye timing diagram



Note (3) Measure point: X –board US0_DT0_P/N~ US12_DT0_P/N

Note (4) Recommended FFC drawing

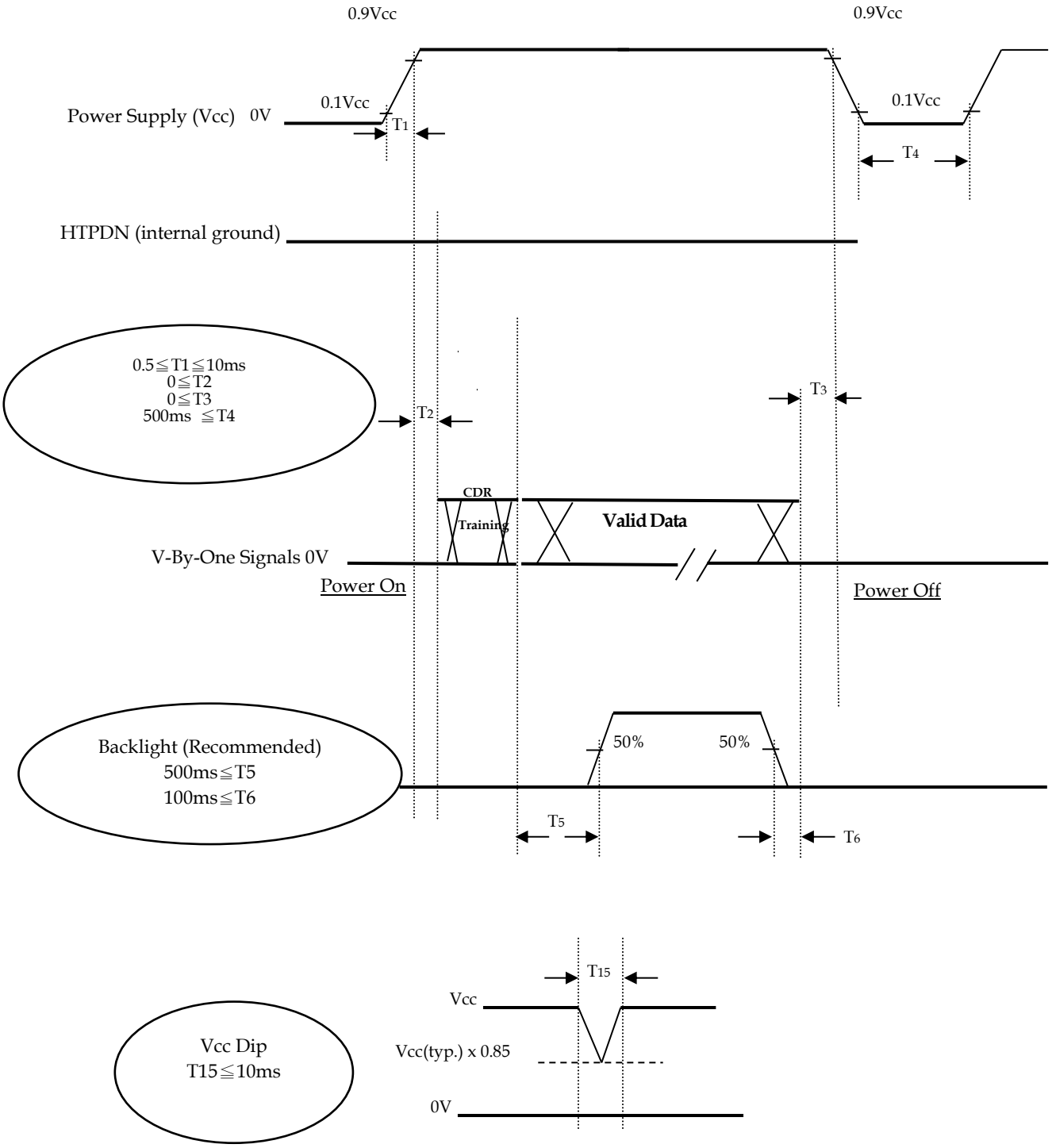


4.5.3 Byte Length and Color mapping of V-by-One HS

Packer input & Unpacker output		30bpp RGB (10bit)
Byte 0	D[0]	R[2]
	D[1]	R[3]
	D[2]	R[4]
	D[3]	R[5]
	D[4]	R[6]
	D[5]	R[7]
	D[6]	R[8]
	D[7]	R[9]
Byte 1	D[8]	G[2]
	D[9]	G[3]
	D[10]	G[4]
	D[11]	G[5]
	D[12]	G[6]
	D[13]	G[7]
	D[14]	G[8]
	D[15]	G[9]
Byte 2	D[16]	B[2]
	D[17]	B[3]
	D[18]	B[4]
	D[19]	B[5]
	D[20]	B[6]
	D[21]	B[7]
	D[22]	B[8]
	D[23]	B[9]
Byte 3	D[24]	X
	D[25]	X
	D[26]	B[0]
	D[27]	B[1]
	D[28]	G[0]
	D[29]	G[1]
	D[30]	R[0]
	D[31]	R[1]

4.5.4 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance besides HTPDN.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) Vcc must be decayed smoothly when power-off.

Note (7) HTPDN (internal ground) : For customer reference signal. It can be ignored if customer not use.

4.6. Input Data Signal, Basic Color and Gray Scale of Each Color (with C-PWB "RUNTK0018HVxx")

Colors & Gray Scale			Data signal																													
			R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	---																														
	---	---																														
	---	GS1021	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1022	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	---																														
	---	---																														
	---	GS1021	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	---	GS1022	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green	GS1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	---	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	---	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	---	---																														
	---	---																														
	---	GS1021	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
	---	GS1022	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Blue	GS1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

- 0: Low level voltage / 1: High level voltage
- Each basic color can be displayed in 1021-gray-scale from 10-bit data signals. According to the combination of total 30-bit data signals, about 1-billion-color display can be achieved on the screen.

5. Optical Characteristics

Ta = 25 ºC, 60 Hz Typical Timing Input to the C-PWB

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range [1]	Horizontal	θ21 θ22	CR ≧ 10	70	88	-	deg.	
	Vertical	θ11 θ12		70	88	-	deg.	
Contrast ratio [2]		CRn	θ = 0 deg.	-	4000	-	-	
Response time [3]		τrd		-	8	-	ms	Temp=30 ºC
Chromaticity	White	Wx		Typ-0.03	0.281	Typ+0.03	-	
		Wy		Typ-0.03	0.297	Typ+0.03	-	
	Red	Rx		Typ-0.03	0.643	Typ+0.03	-	
		Ry		Typ-0.03	0.334	Typ+0.03	-	
	Green	Gx		Typ-0.03	0.303	Typ+0.03	-	
		Gy		Typ-0.03	0.618	Typ+0.03	-	
	Blue	Bx		Typ-0.03	0.153	Typ+0.03	-	
		By		Typ-0.03	0.055	Typ+0.03	-	
Chromaticity (C Light Source)	White	Wx		Typ-0.03	0.303	Typ+0.03		
		Wy		Typ-0.03	0.346	Typ+0.03		
	Red	Rx		Typ-0.03	0.659	Typ+0.03		
		Ry		Typ-0.03	0.324	Typ+0.03		
	Green	Gx		Typ-0.03	0.271	Typ+0.03		
		Gy		Typ-0.03	0.585	Typ+0.03		
	Blue	Bx		Typ-0.03	0.136	Typ+0.03		
		By		Typ-0.03	0.103	Typ+0.03		
Transmittance [4]	White	Tr		-	5.1	-	%	

- Using the C-PWB and the SIO Standard LED Backlight System.
- Measuring after a backlight luminance is stable.
- Gamma Correction, Color-Gradation Correction, and Over-Shoot Driving are valid with the C-PWB
- Measurement equipment is the following,
- Design the backlight in such a way that luminance via TFT-LCD-panel become under 420 cd/m^2 at a maximum. In case the actual luminance condition is higher than above, separate agreement has to be defined based on the evaluation result that both party agreed.

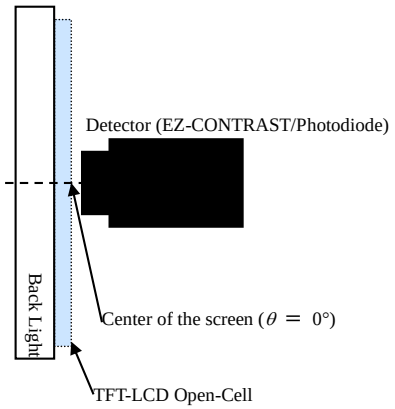


Fig.3-1 Measurement of viewing angle range and Response time.
Viewing angle range: EZ-CONTRAST
Response time: Photodiode

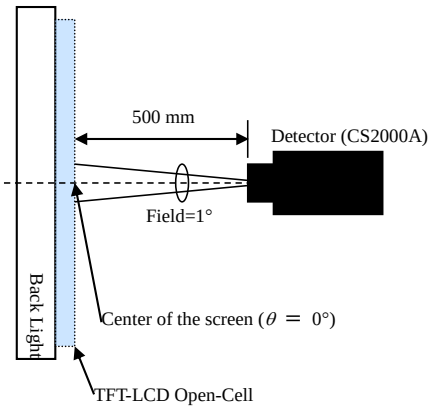


Fig.3-2 Measurement of Contrast, Luminance, Chromaticity and Transmittance.

Fig.3 Optical measuring equipment

1) The viewing angle range is defined as the following,

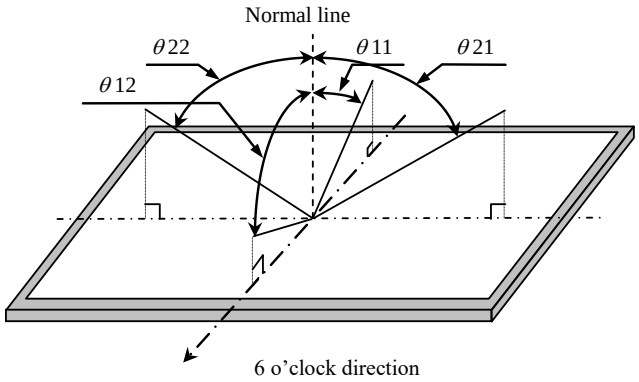


Fig.9 Measurement method of panel transmittance

2) The contrast ratio is defined as the following,

$$\text{Contrast Ratio} = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixelS black}}$$

3) The response time is defined as the following,

$$\tau_{rd} = \{\sum(\tau_r : x - y) + \sum(\tau_d : x - y)\} \Big/ 20$$

τ_{rd} is an average value of a switching time from five luminance levels (0%, 25%, 50%, 75%, and 100%) to five luminance levels (0%, 25%, 50%, 75%, and 100%).

*The following luminance level of 90% specification defines TV-signal (100IRE) level.

		Luminance level of End (y)				
		0%	25%	50%	75%	100%
Luminance level of Start (x)	0%		τ_r : 0%-25%	τ_r : 0%-50%	τ_r : 0%-75%	τ_r : 0%-100%
	25%	τ_d : 25%-0%		τ_r : 25%-50%	τ_r : 25%-75%	τ_r : 25%-100%
	50%	τ_d : 50%-0%	τ_d : 50%-25%		τ_r : 50%-75%	τ_r : 50%-100%
	75%	τ_d : 75%-0%	τ_d : 75%-25%	τ_d : 75%-50%		τ_r : 75%-100%
	100%	τ_d : 100%-0%	τ_d : 100%-25%	τ_d : 100%-50%	τ_d : 100%-75%	

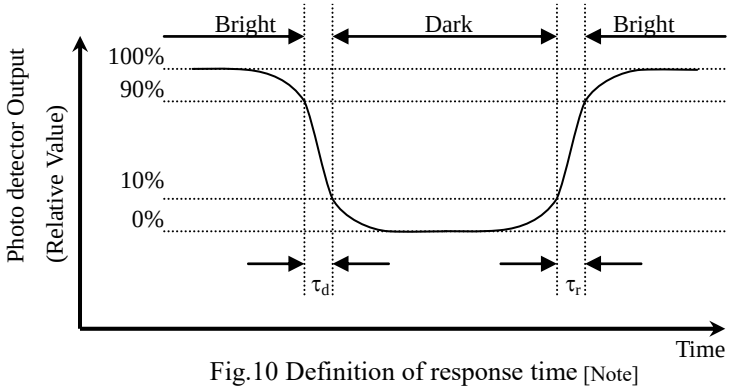


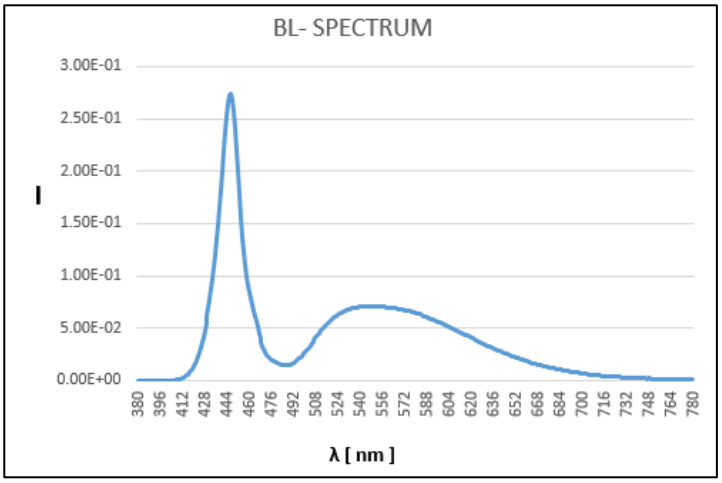
Fig.10 Definition of response time [Note]

[Note] τ_d and τ_r are defined the arrival time from 10% to 90%.

- The average value of before switching :0%
- The average value of after switching :100%

4) The transmittance is defined as the following, Using the SIO Standard (LED) Backlight System

$$\text{Transmittance} = \frac{\text{OpenCell luminance with all pixels white and backlight lighting}}{\text{Backlight luminance}}$$



6. Shipping specification

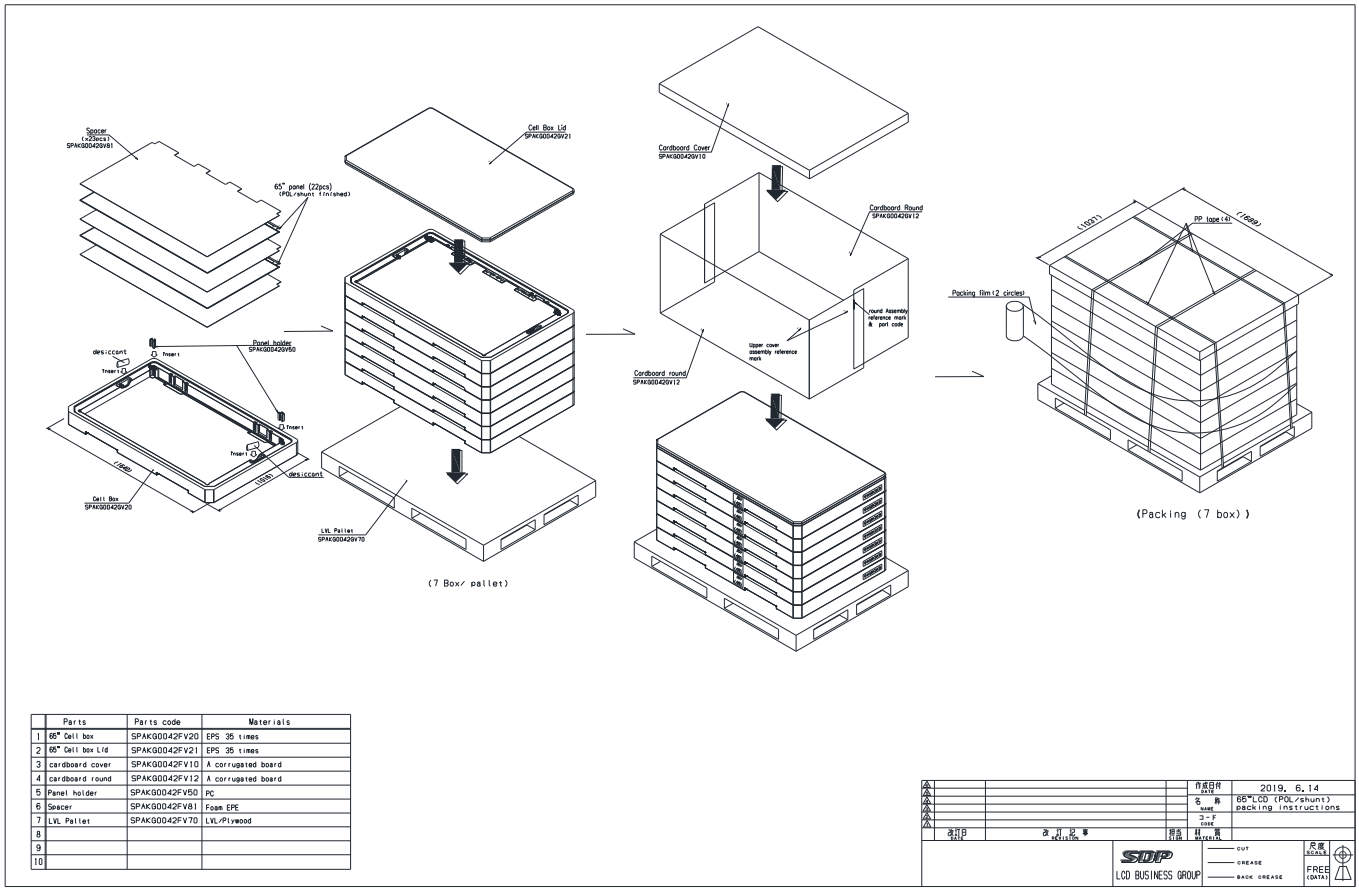
6.1. Packing Form

	1-pallet	1 box
size	1680x1060x1069 (H)[mm]	1640x1016x169 [mm]
Q'ty	154 Open-Cells (7 boxes)	22 Open-Cells
Mass	About 594Kg	About 82.5 Kg

(1) 13 Pcs LCD Panels / 1 Box
(2) Box dimensions : 1640 (L) X 1016 (W) X 169 (H)mm
(3) Weight : approximately 82.5 Kg / 1 Box
(4) 154 PCS LCD TV Panels / 1 Pallet
(5) Group dimensions : 1680 (L) X 1060 (W) X 1069 (H)mm
(6) Weight : approximately 594 Kg / 1 Pallet
(7) Please fill up the container to avoid any cargo be damaged.
(8) SIO recommend to follow the packing method as described in 6.2.
(9) When transferring in warehouse or factory, the arm length of electric forklift or hand pallet truck must be longer than the pallet.
(10) After un-packing, one box is needed to be carried by four persons which is to prevent box bent or fell down.
The surface area of the worktable or carts should be greater than box size.

6.2. Packing Method

(1) Packing Method (EPS Box)



	Parts	Parts code	Materials
1	65" Cell box	SPAKG0042FV20	EPS 35 times
2	65" Cell box Lid	SPAKG0042FV21	EPS 35 times
3	cardboard cover	SPAKG0042FV10	A corrugated board
4	cardboard round	SPAKG0042FV12	A corrugated board
5	Panel holder	SPAKG0042FV50	PC
6	Spacer	SPAKG0042FV81	Foam EPE
7	LVL Pallet	SPAKG0042FV70	LVL/Plywood
8			
9			
10			

		作成日付 DATE	2019. 6. 14
		名 称 NAME	65"LCD (POL/shunt) packing instructions
		コード CODE	
改訂日 DATE	改 訂 記 事 REVISION	担当 DR	材 質 MATERIAL
		SDP LCD BUSINESS GROUP	CUT / CREASE / BACK CREASE
		尺度 SCALE	FREE (DATA)

Figure.4-1 packaging method

(2) Shipping Mode

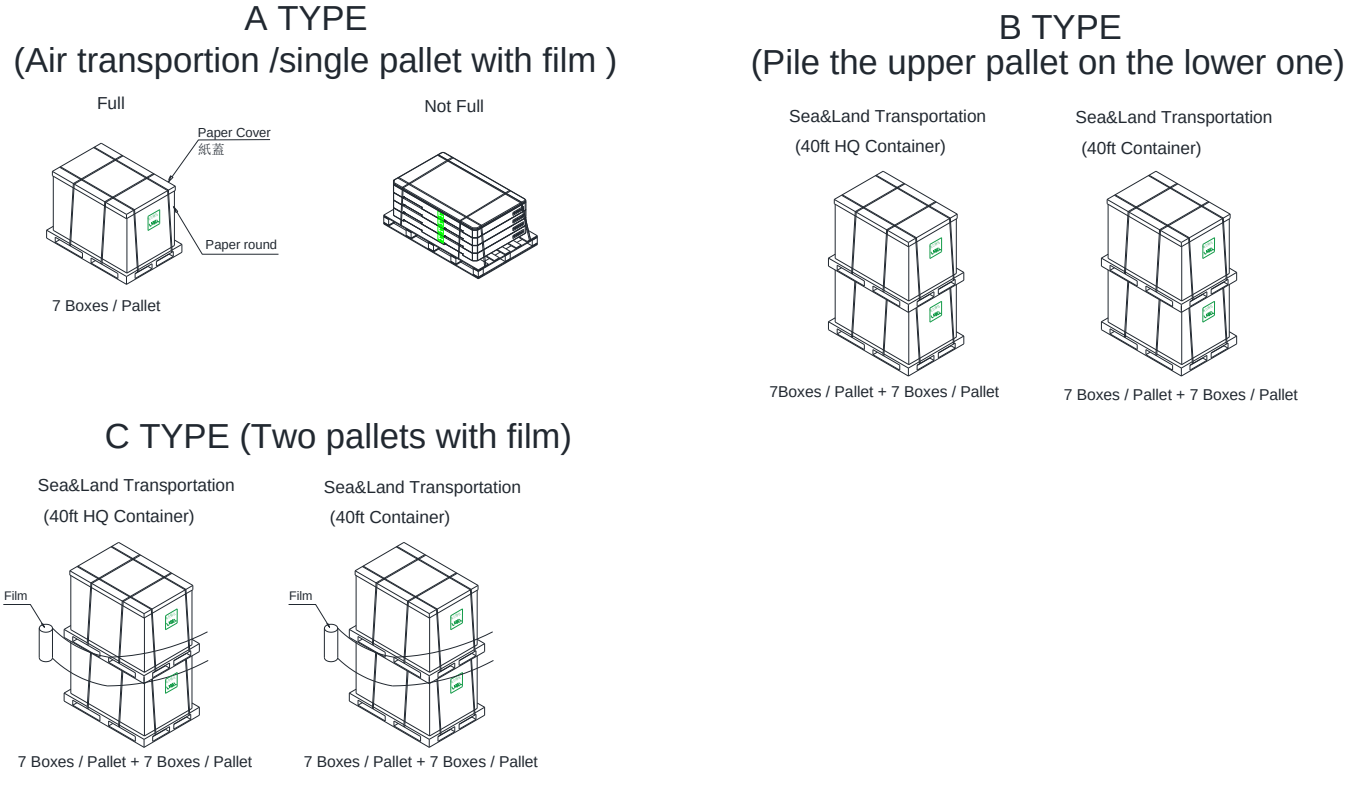


Figure.4-2 shipping mode

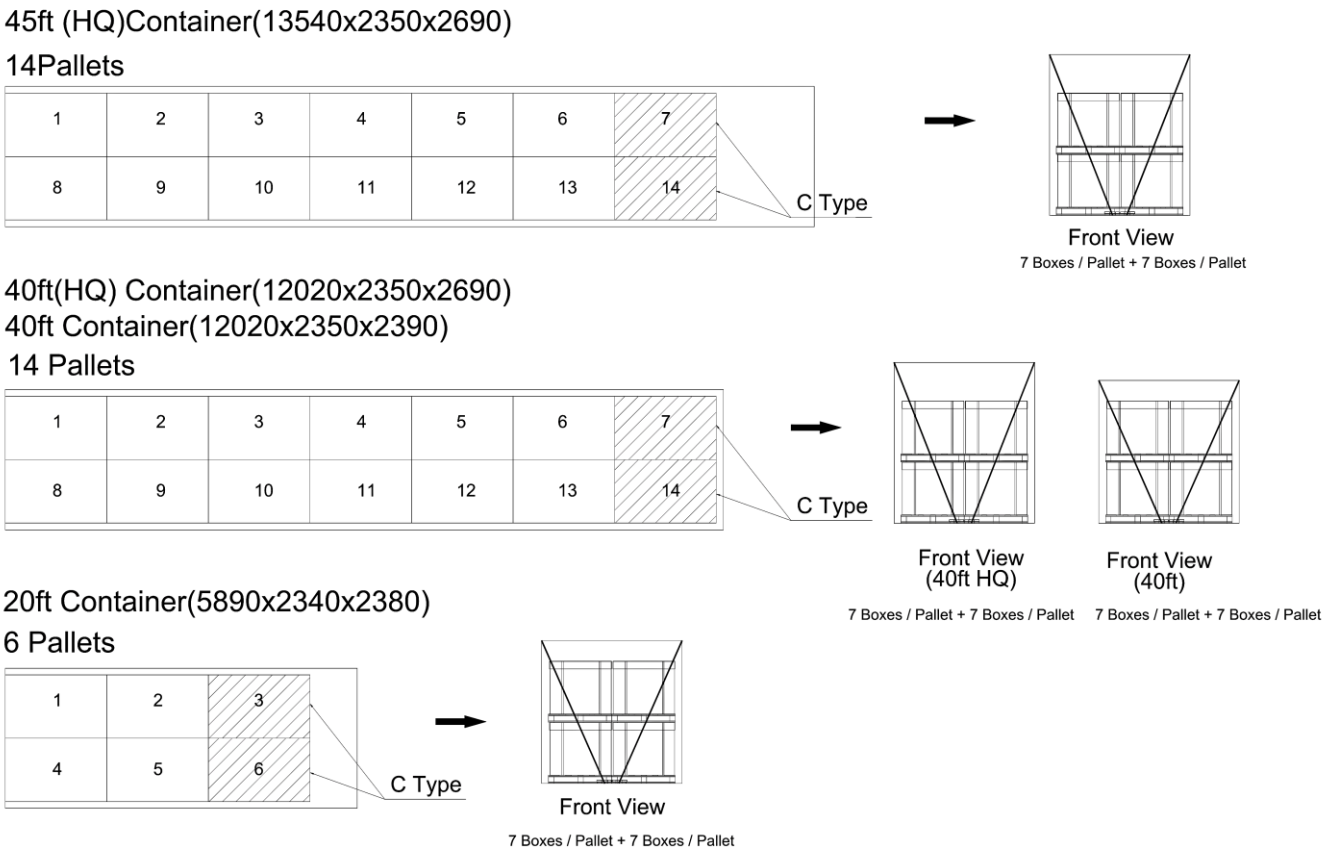
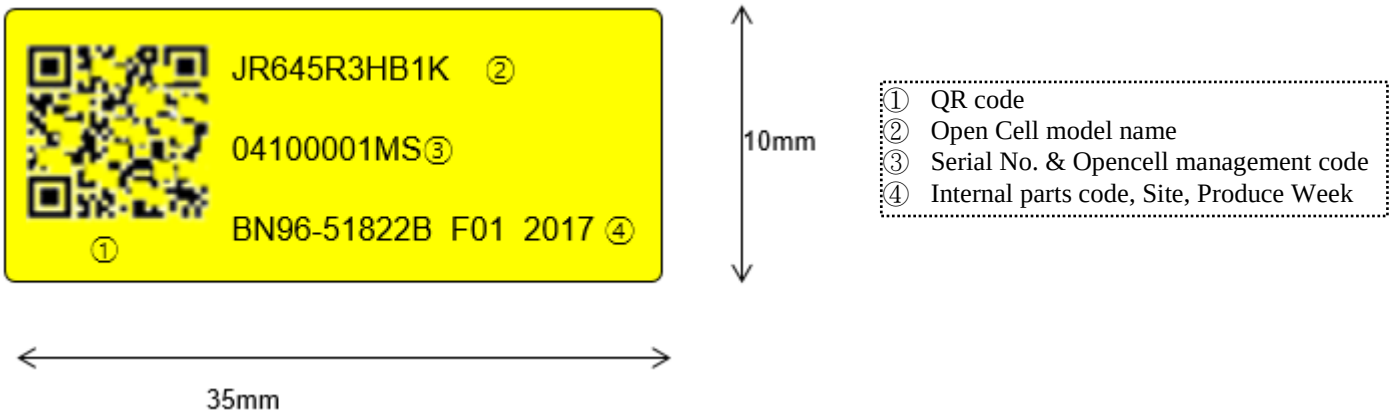


Figure.4-3 shipping mode

6.3. Label

a) Open-Cell Serial Label

This label is pasted on the S-PWB.



① Information in 2D code (QR) code
QR code: Total 38 digits

* 0~9,A~Z,Space

Production name(1-11)+0 (12-14)													
1	2	3	4	5	6	7	8	9	10	11	12	13	14
J	R	6	4	5	R	3	H	B	1	K	0	0	0

Production Date (15-17)+Serial No.(18-22)+Internal code (23-24)+0 (25)										
15	16	17	18	19	20	21	22	23	24	25
Y	M	D	0	0	0	0	1	*	*	0

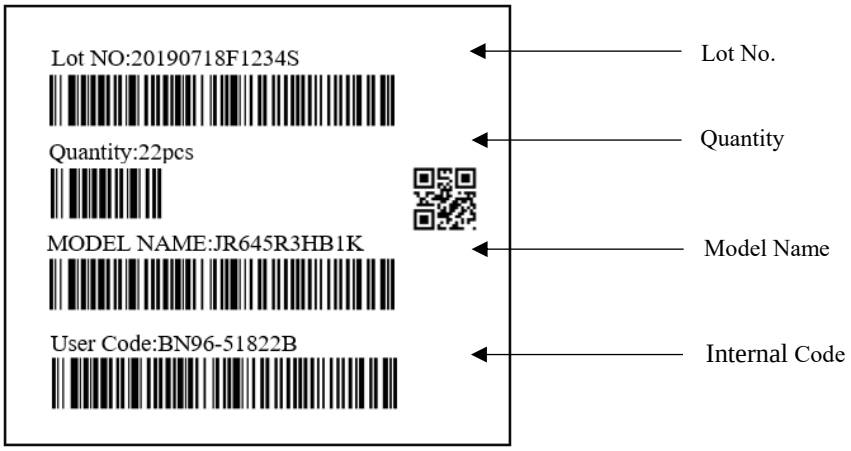
Internal part No.						LCM Site			Produce Week			
26	27	28	29	30	31	32	33	34	35	36	37	38
1	2	3	4	5	A	F	0	2	Y	Y	W	W

②-④ Label printing contents

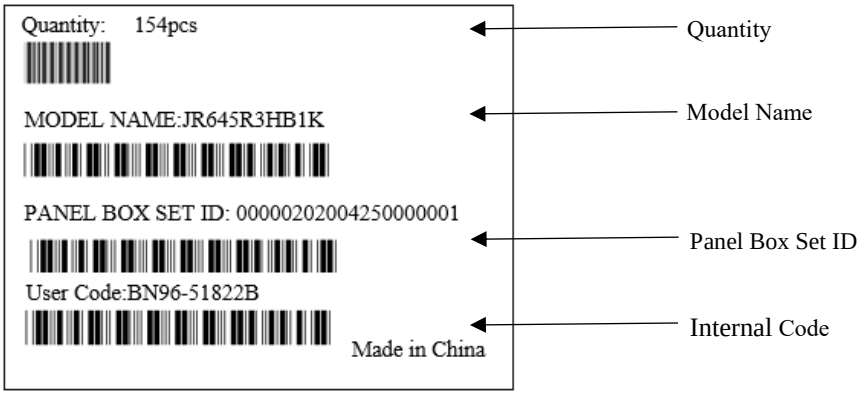
②	Model name: 11 letters
③	Production Date (3 letters) + Serial No. (5 letters)+Opencell management code (2 letters)
④	Internal part No.(11 letters)+Space+Site (3 letters)+Space+Production Week (4 letters)

b) Open Cell Packing Label

·Label on the packing case (cell box)



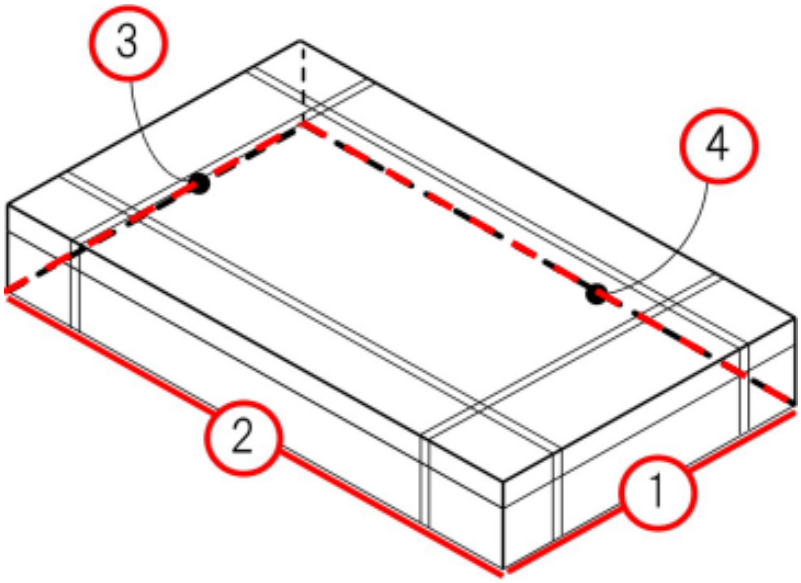
·Label on the packing carton



7. Reliability Test

NO.	Items	Required Condition	Note
1	High Temperature Storage	Ta= 60℃ , 240hrs	
2	Low Temperature Storage	Ta= -20℃ , 240hrs	
3	Temperature Humidity Bias	Ta= 50℃ , 80%RH, 240hrs	
4	Low Temperature Operation	Ta= 0℃ ,240hrs	
5	High Temperature Operation	Ta= 50℃ , 240hrs	
6	Thermal Shock Test	-20℃/30min , 60℃ / 30min , 100 cycles	
7	Packing Vibration	Z axis 60 min，X/Y axis each 15min(Spectrum 5~50Hz 9.8m/s2(1G))	
8	Packing Drop	Height = 15cm for 4 sides each one time	

- Note (1) Criteria : Normal display image with no obvious non-uniformity and no line defect
- Note (2) Evaluation should be tested after storage at room temperature for more than two hour
- Note (3) Packing Drop test 4 side as below



8. International Standards(Environment)

RoHS Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU of the European Parliament and of the council.

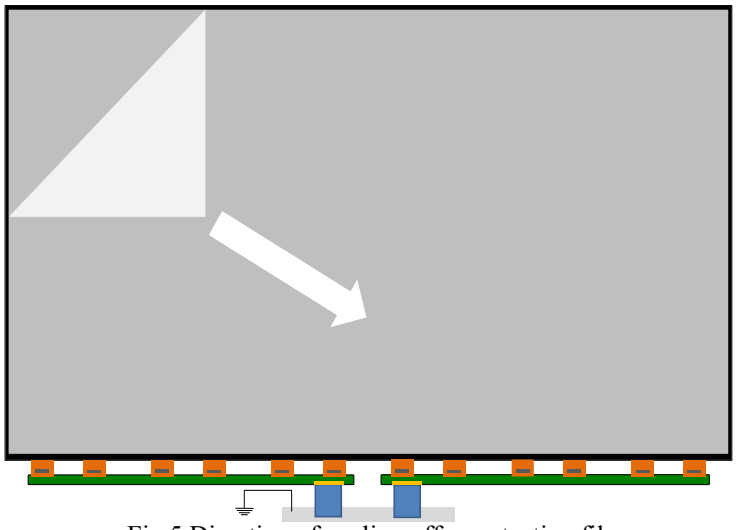
9. Precautions

a) Since this Open-Cell consists of TFTs and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharges, persons who are handling the Open-Cell should be grounded through adequate methods such as the anti-static wrist band. Connector pins should not be touched directly with bare hands.

- Reference : Process control standard of SIO

	Item	Management standard value and performance standard
1	Anti-static mat (shelf)	1 to 50 [Mohm]
2	Anti-static mat (floor, desk)	1 to 100 [Mohm]
3	Ionizer	Attenuate from ±1000 V to ±100 V within 2 sec
4	Anti-static wrist band	0.8 to 10 [Mohm]
5	Anti-static wrist band entry and ground resistance	Less than 1000 ohm
6	Temperature	22 to 26 [ºC]
7	Humidity	60 to 70 [%]

b) This Open-Cell is with the Protection Film on Polarizers. Please take care following notices within the removal of protection films.



- Be sure to peel off slowly (recommended more than 17 sec) and constant speed.
- Peeling direction shows Fig.
- Be sure to ground person with adequate methods such as the anti-static wrist band.
- Be sure to ground all terminals of the S-PWB while peeling of the protection film.
- Ionized air should be blown over during peeling action.
- The protection film must not touch drivers and S-PWBs.
- If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.

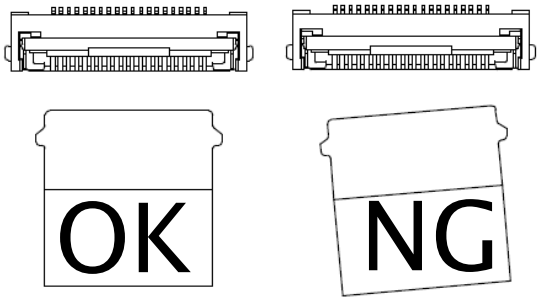
Fig.5 Direction of peeling off a protection film

c) Since the polarizer is easily damaged, pay attention not to scratch it.
d) When the polarizer is soiled, wipe it with the absorbent cotton or other soft cloth.
e) Since this TFT-LCD-panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.
f) When this TFT-LCD-panel surface gets strong pressures locally by being hit or pressed strongly by something, display Mura might remain permanently at the area where such pressures are applied. Do not push or hit by the power beyond 10N for active area of display.
g) For GOA circuit part, do not push or hit the power beyond 2.5kg/cm^2 and avoid continuous force more than 30 seconds.
h) Since the TFT is shifted a threshold with photo excitation, shade the outside of the back polarizer from the backlight.
i) There is a common electrode with the CF Glass Edge of this TFT-LCD Panel. Do not touch the CF Glass Cut Line with conductive materials since an abnormal display may occur.
j) Please don't warp or twist the TFT-LCD-panel at handling and be sure to use suction jig at handling of the Open-Cell to prevent any external damage including warpage, cosmetic dirt and scratch.

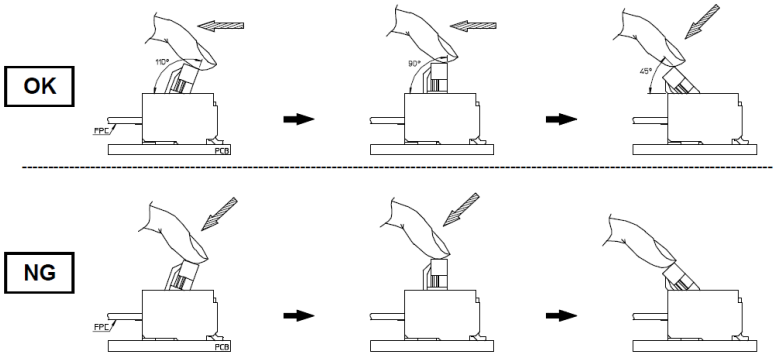
Note: This limit is only for a short time at handling of the TFT-LCD-panel.
The module and cabinets need to be designed not to add extra stress to the TFT-LCD-panel that cause warp or twist.

Fig.6 Limit of warpage at handling of panel

k) This Open-Cell has some PWBs, take care to keep them from any stress or pressure when handling or installing the Open-Cell, otherwise some of electronic parts on the PWB may be damaged.
l) To prevent the disconnection of S-SOFs by the thermal shock or physical damage, design the module not to fix S-PWBs with screws or tape.
m) When handling the Open-Cell and assembling them into cabinets, be noted that a long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the Open-Cell.
n) Applying too much force and stress to PWBs and SOFs may cause a malfunction electrically and mechanically.
o) In case that the SOF is needed to bend, note that the radius of bending have to be over 0.65 mm in 2 mm outside from the Driver-IC edge.
p) To radiate a heat of Source-Driver-IC(S-IC) s, the recommended operating maximum temperature is 125 ºC at a chip surface, design the module to contact the opposite side of S-ICs with a high thermal conductivity material.[Fig.13-1]
q) Handle with care based on the general connector's specification when inserting and removing FFCs or FPCs.
r) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.
s) Turn off the power supply when inserting or disconnecting the cable.
t) This Open-Cell has high frequency circuits. Sufficient suppression to EMI should be done by system manufacturers.
u) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.
v) The chemical compound, which causes the destruction of ozone layer, is not being used.
w) Instruction of connector upon usage.
   a) Do with the actuator opened completely, and insert it in the interior of the insertion entrance surely horizontally when you insert FFC or FPC. (Please put the FFC or FPC tab in the ditch of the housing surely with the FFC or FPC tab.) Might it become short defective, and it causes the corner to transform the caught terminal into the terminal by the pitch gap when inserting it right and left and diagonally.

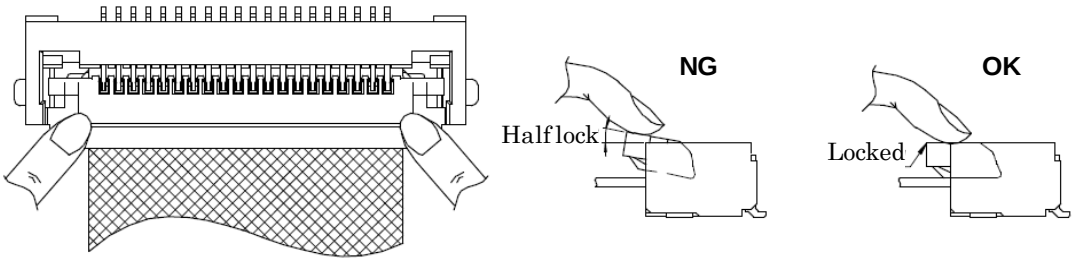


b) Please add force in the direction where the actuator is held and do by rotating it pushing in parallel to the C-PWB direction when becoming 90°or less as shown in the figure below until the angle of the actuator becomes 90°or less when you shut the actuator. Please do not add the force to rotary axis of actuator in the direction that the actuator is off.



c) About the lock operation

When you lock, it should be push on both sides of the actuator. And it is necessary to confirm that the actuator is surely shut.



x) This Open-Cell is corresponded to RoHS. “R.C.” label on the side of a palette shows it.
y) When any question or issue occurs, it shall be solved by mutual discussion.
z) Be sure to design the LCD module and cabinet not to bend the S-SOF at the unbendable area [Fig. 13-2] to avoid the disconnection of wires or removal of IC chip from film.
aa) In case that S-SOF are needed to bend, please note that the radius of bending have to be over 0.65 mm [Fig. 13-2].

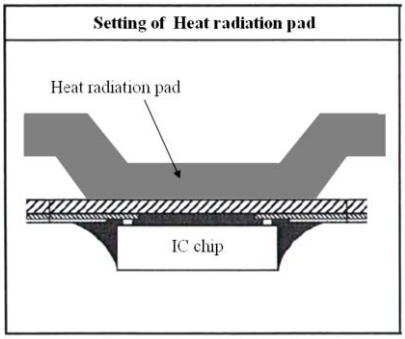


Fig.7-1 Diagram of setting example of Heat radiation pad on S-SOF

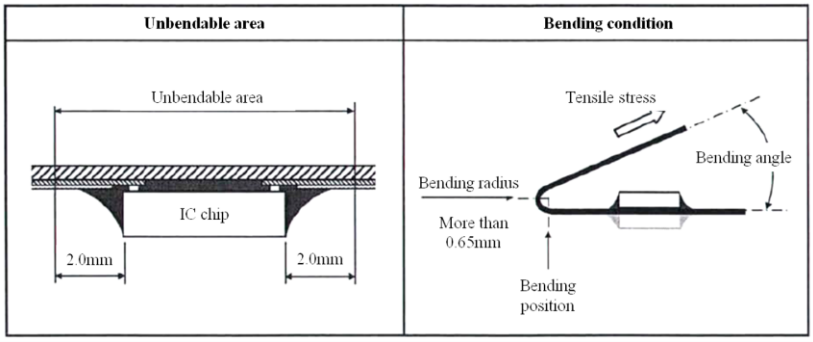


Fig.7-2 Unbendable area and Bending condition of S-SOF

bb) Be sure to design the LCD module and cabinet not to fix with SPWB by screws to prevent the disconnection of S-SOF by the thermal shock or physical damage.
cc) When the panel surface gets the strong pressure locally by being hit or pressed strongly by something, display Mura might

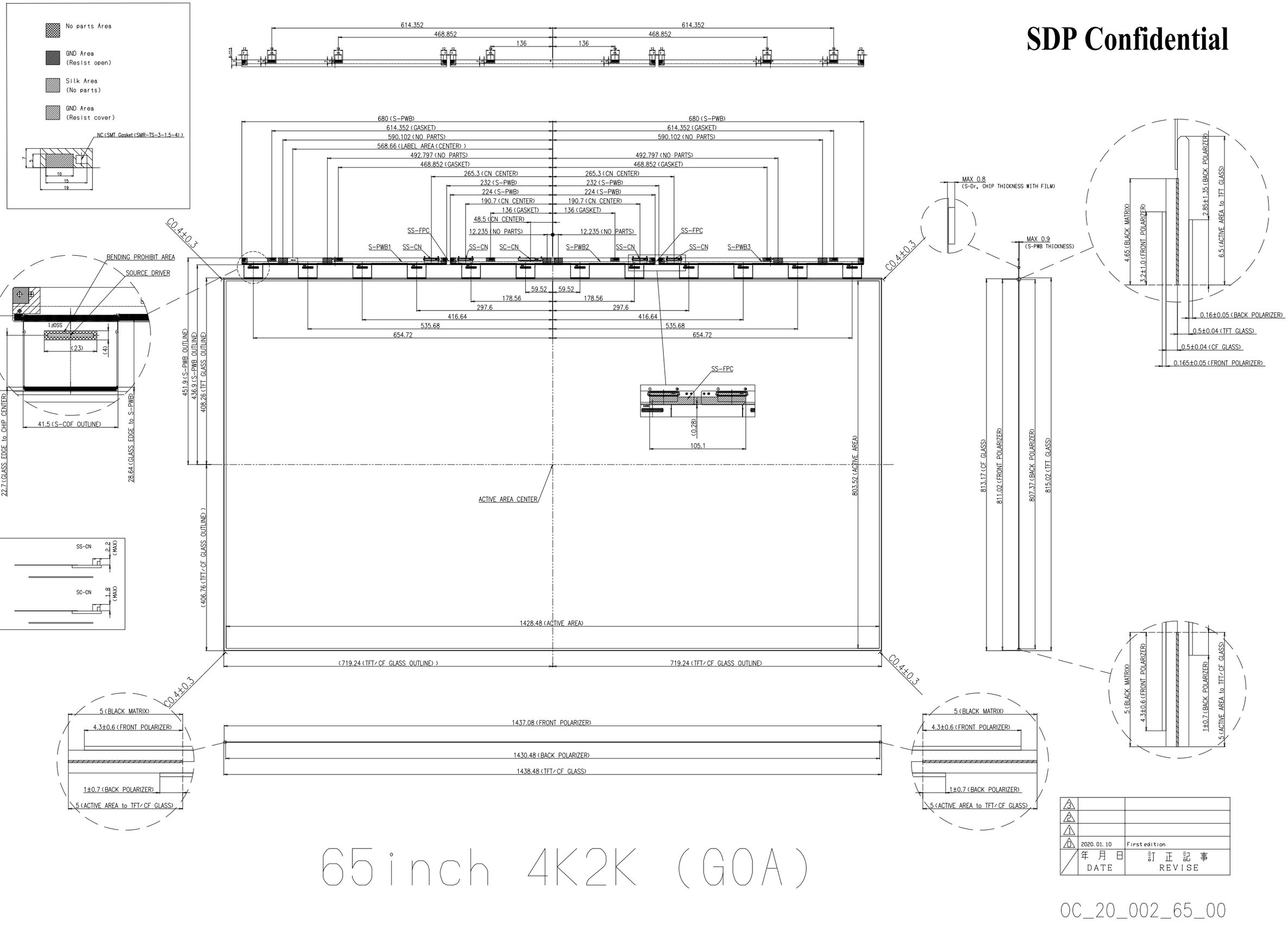
remain permanently at the area where such pressure is applied. Therefore, please be careful well of handling panel in your production process and also call end customer attention for careful handling.

dd) Since damage may be done from the sticker within permission, please do not use the corner edge of a panel for positioning use or holding a panel.

ee) Since there is possibility of injury with the panel edge, please design the TV set so that the user can not touch the panel edge.

10. Storage Conditions of Open-Cell in Cell-Box

-	Temperature	0 ºC to 40 ºC
-	Humidity	95% RH or less
-	Reference condition	20 ºC to 35 ºC, 85% RH or less (summer) 5 ºC to 15 ºC, 85% RH or less (winter) The total storage time (40 ºC, 95%RH) : 240 hours or less
-	Sunlight	Shelter a production from the direct sunlight.
-	Atmosphere	Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
-	Notes	Put the box on a pallet or a base, do not put it on a floor, and store them with removing from a wall. Take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment.
-	Storage life	1 year



65inch 4K2K (GOA)

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