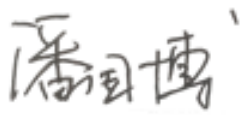
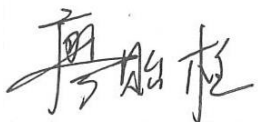
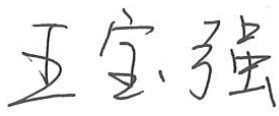
TITLE : HV550QUB-F1D

Open Cell Specification

Rev.O

Customer : LGE

APPROVED BY	
DATE	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Fuzhou BOE Optoelectronics Technology Co., Ltd

REVISION HISTORY

( )preliminary specification
(√)Final specification

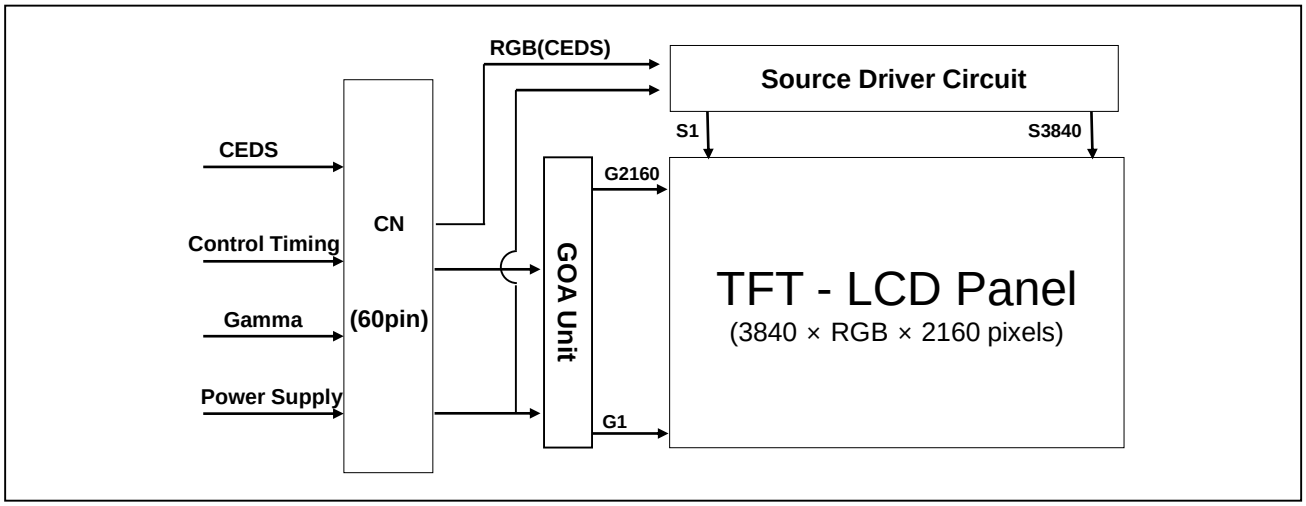
Revision No.	Page	Description of changes	Date	Prepared
P0	Total Page	Initial Release	2021.03.18	XQ Zhang
P1	P10/11	Update power consumption and optical spec	2021.04.19	XQ Zhang
P2	P7/8/32-36	Update Voltage range spec Update TBD items	2021.04.25	XQ Zhang
O	Total Page	Final Release Update VGH margin	2021.06.09	XQ Zhang

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

HV550QUB-F1D is a color active matrix TFT LCD open cell using amorphous silicon TFT‘s (Thin Film Transistors) as an active switching devices. This module has a 55 inch diagonally measured active area with UHD resolutions (3840 horizontal by 2160 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 1.07G colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



1.2 Features

- CEDS interface with 6 pairs
- High-speed response
- Low color shift image quality
- 8-bit + FRC color depth, display 1.07G colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- Gate driver use GOA mode
- ADS technology is applied for high display quality
- RoHS compliant

1.3 Application

- Home Alone Multimedia TFT-LCD TV only
- Ultra High Definition TV(UHD TV)
- Display Terminals for Control System, Public Monitor and etc… are not allowed

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Active area	1209.6(H) × 680.4(V)	mm	
Number of pixels	3840*(RGB)*2160	pixels	
Pixel pitch	105(H) × 3(RGB) ×315(V)	㎛	
Pixel arrangement	Pixels RGB Island	-	
Display colors	1.07G (8bits + FRC)	colors	8bit driver IC
Display mode	Transmission mode, Normally Black		
Open Cell Transmittance	5.2(Typ.)	%	At center point with BOE BLU
Weight	2700(Typ.)	gram	
Power Consumption	12(Typ.)	Watt	With TCON board
Surface Treatment	Haze 1%, 2H(Min), Anti-glare treatment (Front Polarizer) Clear(Bottom Polarizer)	-	

2.0 ABSOLUTE MAXIMUM RATINGS

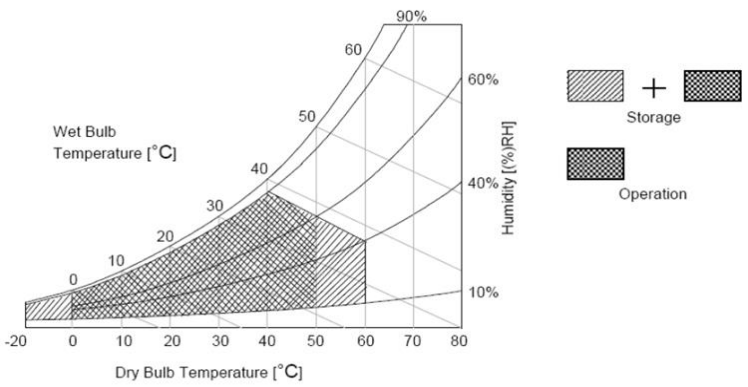
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit.

< Table 2. Open Cell Absolute Maximum Ratings >

Parameter	Symbol	Min.	Max.	Unit	Remark
Operating Temperature	T_{OP}	0	+50	℃	Note 1 Note 2
Storage Temperature	T_{SUR}	-20	+60	℃	
	T_{ST}	-20	+60	℃	
Panel Surface Temperature (Considering LC phase Transition)	T_{PT}	-	+65	℃	
Operating Ambient Humidity	Hop	10	90	%RH	
Storage Humidity	Hst	10	90	%RH	
Logic & CEDS Power Voltage	VDD	-0.3	+2.5	V	
Gate High Voltage	VGH	+20.0	+40	V	
Gate Low Voltage	VGL	-12	-5.5	V	
Source D-IC Analog Voltage	AVDD	-0.3	+20.0	V	
Gamma Ref. Voltage (Upper)	Pos.	HAVDD	AVDD	V	
Gamma Ref. Voltage (Low)	Neg.	0	HAVDD	V	

Note 1 : Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ℃ max. and no condensation of water.

Note 2 : Thermal management should be considered in terminal product design to prevent the surface temperature of display area from being over 65℃.The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65℃ with LCD module alone in a temperature controlled chamber.



3.0 ELECTRICAL SPECIFICATIONS

3.1 Open Cell Electrical Specifications

< Table 3. Open Cell Voltage Setting Specifications > [Ta =25±2 ℃]

Characteristics	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	DVDD1V8S	1.73	1.88	1.98	V
DC Supply Voltage	VGL	-6.2	-6.0	-5.8	V
DC Supply Voltage	LVGL	-6.2	-6.0	-5.8	V
DC Supply Voltage	VGH	35	36	38	V
DC Supply Voltage	VCOM	6.94	7.44	7.94	V
DC Supply Voltage	HAVDD	7.8	8.0	8.2	V
DC Supply Voltage	AVDD	17.4	17.6	17.8	V
DC Supply Voltage	GMA1	15.45	15.7	15.95	V
DC Supply Voltage	GMA3	13.36	13.56	13.76	V
DC Supply Voltage	GMA5	11.75	11.95	12.15	V
DC Supply Voltage	GMA9	8.35	8.5	8.65	V
DC Supply Voltage	GMA10	7.35	7.5	7.65	V
DC Supply Voltage	GMA14	3.9	4.05	4.2	V
DC Supply Voltage	GMA16	2.28	2.43	2.58	V
DC Supply Voltage	GMA18	0.2	0.3	0.4	V

Notes:
1. VTERM: For CML Mode only, LVDS Mode keeps NC. LVDS Mode S-IC logic power needs 1.8V only, CML Mode S-IC logic power needs 1.8V and VTERM needs 1.2V.
2. VGH should be tested on SOC board. High voltage of STV/CLK/VDDODD/VDDEVEN is as same as VGH voltage.
3. Other test points are on source board. Use typical pattern to test.

3.1 Open Cell Electrical Specifications

< Table 4. Open Cell Current Setting Specifications > [Ta =25±2 ℃]

Characteristics	Symbol	Min	Typ	Max	Unit
DC Supply Current	DVDD1V8S	-	-	240	mA
DC Supply Current	VGL	-	-	20	mA
DC Supply Current	LVGL	-	-	80	mA
DC Supply Current	VGH	-	-	120	mA
DC Supply Current	VCOM	-	-	20	mA
DC Supply Current	HAVDD	-	-	20	mA
DC Supply Current	AVDD	-	-	830	mA
DC Supply Current	GMA1	-	-	20	mA
DC Supply Current	GMA2	-	-	20	mA
DC Supply Current	GMA3	-	-	20	mA
DC Supply Current	GMA4	-	-	20	mA
DC Supply Current	GMA5	-	-	20	mA
DC Supply Current	GMA6	-	-	20	mA
DC Supply Current	GMA7	-	-	20	mA
DC Supply Current	GMA8	-	-	20	mA
DC Supply Current	GMA9	-	-	20	mA
DC Supply Current	GMA10	-	-	20	mA
DC Supply Current	GMA11	-	-	20	mA
DC Supply Current	GMA12	-	-	20	mA
DC Supply Current	GMA13	-	-	20	mA
DC Supply Current	GMA14	-	-	20	mA
DC Supply Current	GMA15	-	-	20	mA
DC Supply Current	GMA16	-	-	20	mA
DC Supply Current	GMA17	-	-	20	mA
DC Supply Current	GMA18	-	-	20	mA

Notes:
1. Current is RMS value test with TCON board; The input current drive capability must more than the Max v alue.
2. VCOM short-circuit current is 400mA.
3. VGH should be tested on SOC board.
4. Other test points are on SOC board. Use maximum pattern to test.

3.1 Open Cell Electrical Specifications

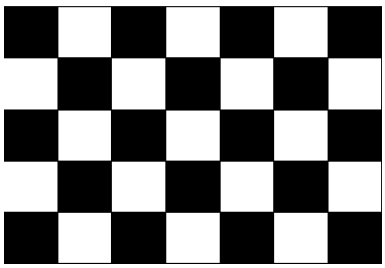
< Table 5. Open Cell Voltage Ripple Specifications > [Ta =25±2 ℃]

Characteristics	Symbol	Max	Unit
DC Supply Ripple	DVDD1V8S	±5%	mV
DC Supply Ripple	VGL	±5%	mV
DC Supply Ripple	LVGL	±5%	mV
DC Supply Ripple	VGH	±5%	mV
DC Supply Ripple	VCOM	±5%	mV
DC Supply Ripple	HAVDD	±5%	mV
DC Supply Ripple	AVDD	±5%	mV
DC Supply Ripple	GMA1	400	mV
DC Supply Ripple	GMA2	400	mV
DC Supply Ripple	GMA3	300	mV
DC Supply Ripple	GMA4	300	mV
DC Supply Ripple	GMA5	300	mV
DC Supply Ripple	GMA6	300	mV
DC Supply Ripple	GMA7	300	mV
DC Supply Ripple	GMA8	300	mV
DC Supply Ripple	GMA9	300	mV
DC Supply Ripple	GMA10	300	mV
DC Supply Ripple	GMA11	300	mV
DC Supply Ripple	GMA12	300	mV
DC Supply Ripple	GMA13	200	mV
DC Supply Ripple	GMA14	200	mV
DC Supply Ripple	GMA15	150	mV
DC Supply Ripple	GMA16	150	mV
DC Supply Ripple	GMA17	50	mV
DC Supply Ripple	GMA18	50	mV

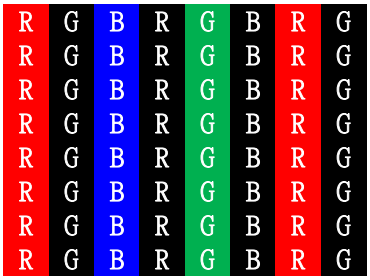
Notes:
1. Voltage ripple is Vpeak to Vpeak value. The ripple does not include V-blanking area ripple.
2. VGH should be tested on SOC board.
3. Other test points are on source board. Use maximum pattern to test.

3.2 Power Consumption and Flicker Pattern

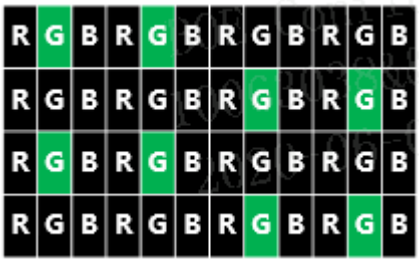
a) Typ : Mosaic 7X5 (L0/L255)



b) Max : Vertical Sub Line (L0/L255)



c) Flicker Test Pattern



Parameter	Symbol	Min	Typ	Max	Unit
Power Consumption	PDD	-	12	26	W
Power Supply Current	IDD	-	1000	2166	mA

Notes : Power consumption & current were measured by BOE T/con board.
Input Voltage was 12.0V

3.3 Driver Characteristics

< Table 6. Driver Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
Driver Surface Temperature	T_{DS}	-	-	125	℃	Note

Note 1: Any point on the driver surface must be less than 125 ℃ under any conditions.
2: This test condition is based on BOE module.

4.0 OPTICAL SPECIFICATION

The test of optical specifications shall be measured in a dark room (ambient luminance≤1 lux and temperature=25±2℃) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V +/-10% at 25°C. Optimum viewing angle direction is 6 'clock.

< Table 7. Optical Table >

[VDD = 12.0V, Frame rate = 60Hz, Ta =25±2 ℃]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10	-	89	-	Deg.	Note1
		Θ_9		-	89	-	Deg.	
	Vertical	Θ_{12}		-	89	-	Deg.	
		Θ_6		-	89	-	Deg.	
Contrast ratio		CR	Θ = 0° (Center) Normal Viewing Angle	1000	1200	-		Note2
Reproduction of color	White	W_x		TYP. - 0.03	0.269	TYP. + 0.03		Note3
		W_y			0.284			
	Red	R_x			0.643			
		R_y			0.340			
	Green	G_x			0.304			
		G_y			0.617			
	Blue	B_x			0.154			
		B_y			0.056			
Response Time	G to G	T_g		-	8	10	ms	Note4
Cell Transmittance				4.68	5.2	-	%	Note5
Gamma Scale				2.0	2.2	2.4		

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of $\theta = 0°$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in this table shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. The chromaticity coordinates are based on BOE backlight.
4. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV = 60Hz with BOE Tcon Board to optimize. Each time in below table shall be measured by switching the input signal for "any level of gray(bright)"and "any level of gray(dark)"

Measured Response Time		Target																
		0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
Start	0																	
	15																	
	31																	
	47																	
	63																	
	79																	
	95																	
	111																	
	127																	
	143																	
	159																	
	175																	
	191																	
	207																	
	223																	
	239																	
	255																	

5. Definition of Transmittance (T%) :
   Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100\ \%$$

Notes :

6. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)
L0	0.00%
L1	0.00%
L31	0.97%
L63	4.61%
L127	21.58%
L191	52.95%
L223	74.45%
L254	99.14%
L255	100.00%

Notes : P-Gamma applied the Typical spec.

5.0 INTERFACE CONNECTION

5.1 Connector Pin Configuration

< Table 8. Open Cell XPCBL Input Connector Pin Configuration >

PIN	Left
1	NC
2	NC
3	NC
4	NC
5	GND
6	GMA18
7	NC
8	GMA14
9	GMA13
10	GMA10
11	GMA9
12	GMA6
13	GMA5
14	NC
15	GMA1
16	GND
17	LOCKOUT6
18	GND
19	CEDS6-
20	CEDS6+
21	GND
22	CEDS5-
23	CEDS5+
24	GND
25	CEDS4-
26	CEDS4+
27	GND
28	NC
29	NC
30	GND
31	LOCKOUT3
32	VCC_12
33	VCC_18
34	VCC_18
35	HVDD
36	VDD
37	VDD
38	VDD
39	VDD
40	GND
41	VCOM1
42	NC
43	NC
44	P_VGL
45	STV
46	NC
47	LS_VGL
48	VGH_EVEN
49	VGH_ODD
50	NC
51	CLK10
52	CLK9
53	CLK8
54	CLK7
55	CLK6
56	CLK5
57	CLK4
58	CLK3
59	CLK2
60	CLK1

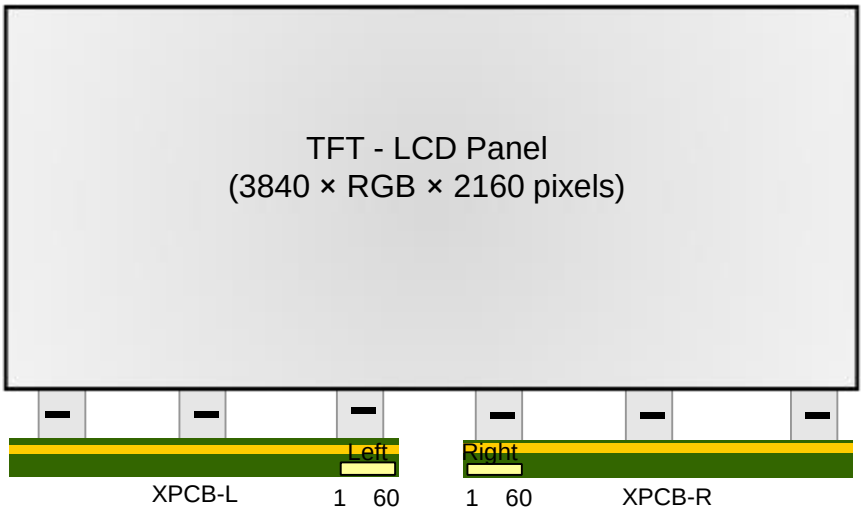
5.1 Connector Pin Configuration

< Table 9. Open Cell XPCBR Input Connector Pin Configuration >

PIN	Right
1	CLK1
2	CLK2
3	CLK3
4	CLK4
5	CLK5
6	CLK6
7	CLK7
8	CLK8
9	CLK9
10	CLK10
11	NC
12	VGH_ODD
13	VGH_EVEN
14	LS_LGL
15	NC
16	STV
17	P_VGL
18	NC
19	NC
20	VCOM1
21	GND
22	VDD
23	VDD
24	VDD
25	VDD
26	HVDD
27	VCC_18
28	VCC_18
29	VCC_12
30	LOCKOUT3
31	GND
32	NC
33	NC
34	GND
35	CEDS3-
36	CEDS3+
37	GND
38	CEDS2-
39	CEDS2+
40	GND
41	CEDS1-
42	CEDS1+
43	GND
44	GMA18
45	NC
46	GMA14
47	GMA13
48	GMA10
49	GMA9
50	GMA6
51	GMA5
52	NC
53	GMA1
54	NC
55	NC
56	NC
57	NC
58	GND
59	NC
60	NC

Notes :

1. NC (Not Connected) : These pins show status of T/con board and are only used for BOE internal operations.
2. XPCBL and XPCBR Input pins assignments refer to the below diagram.

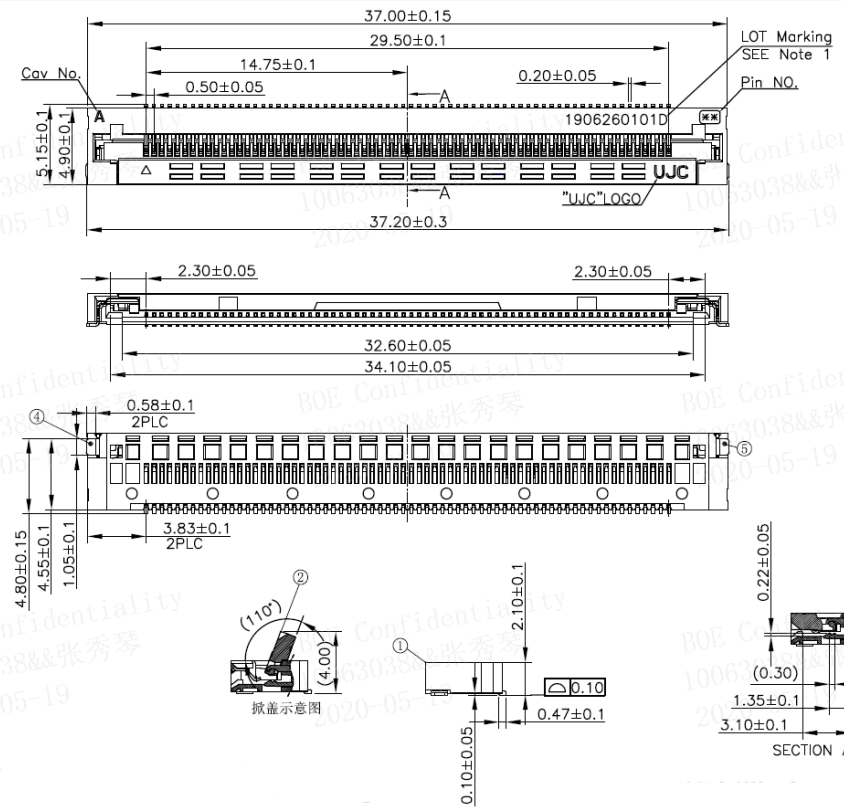


3. VTERM pin is used for CEDS CML mode only. This product supports CML mode and LVDS mode. Keep this pin NC when using LVDS mode.

5.0 INTERFACE CONNECTION

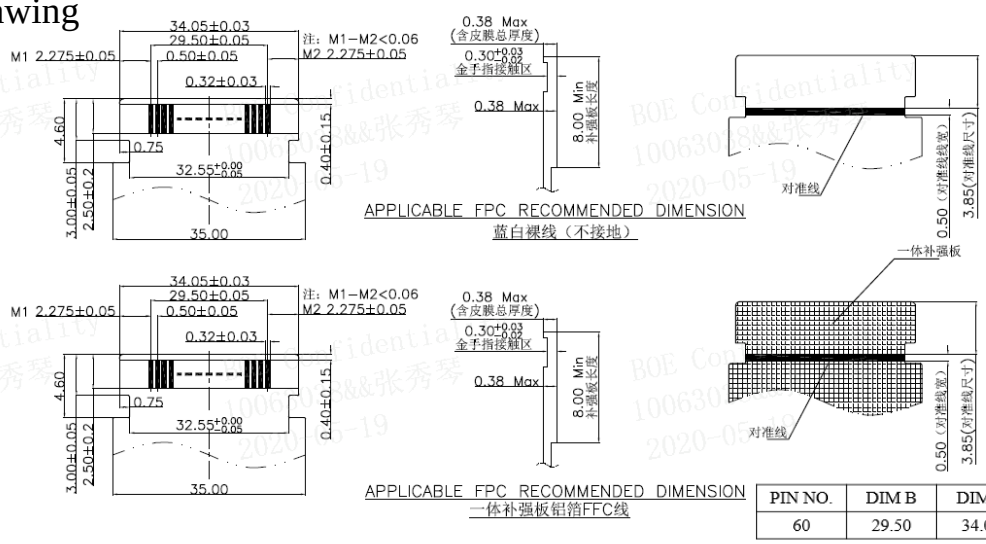
5.1 Open Cell Input Connector & FFC Drawing

-60pin Connector Drawing-PM.FPC.LVS4906001 (UJC)



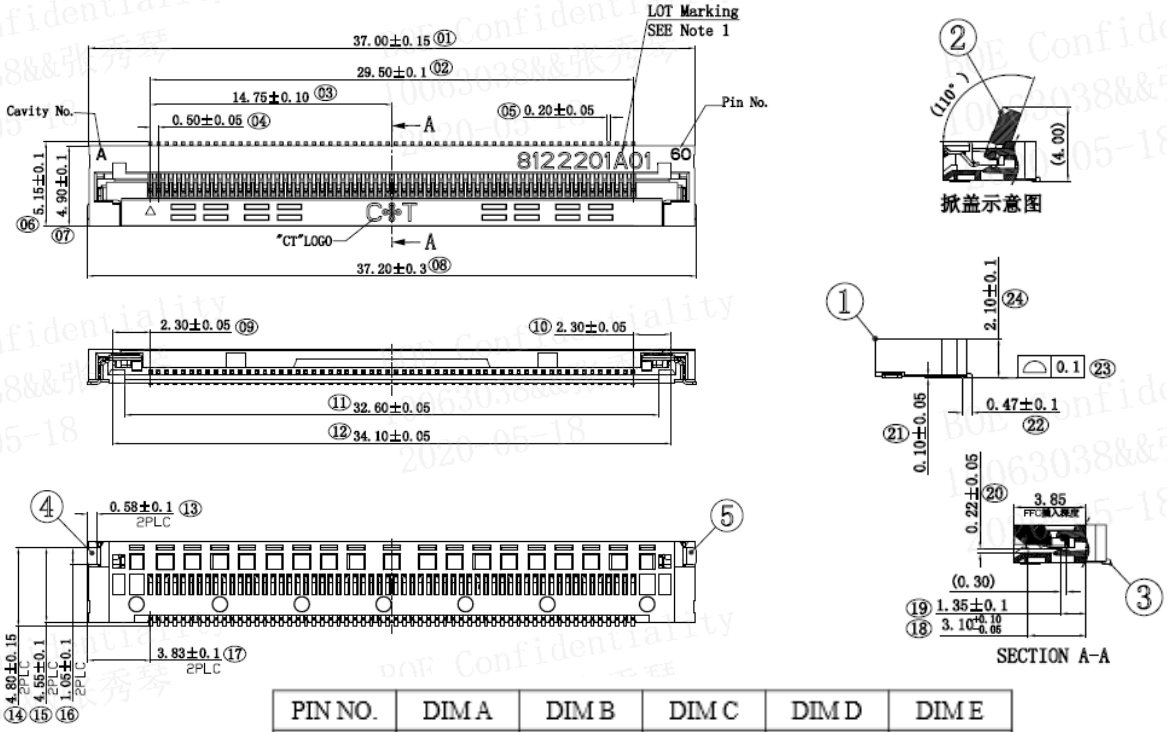
PIN NO.	DIM A	DIM B	DIM C	DIM D	DIM E
60	37.00	29.50	37.20	34.10	32.60

- FFC Drawing



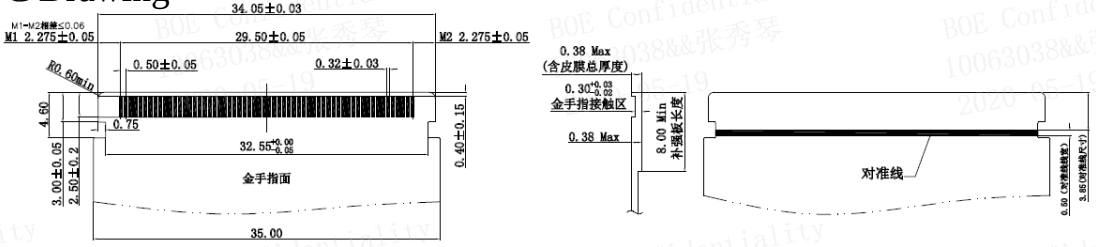
PIN NO.	DIM B	DIM E	DIM F	DIM G
60	29.50	34.05	35.00	32.55

-60pin Connector Drawing-F05049-60P-H (Changtong)

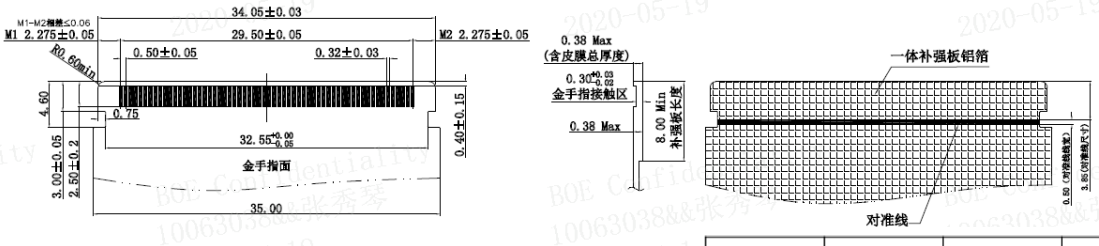


PIN NO.	DIM A	DIM B	DIM C	DIM D	DIM E
60	37.00	29.50	37.20	34.10	32.60

- FFC Drawing



APPLICABLE FPC RECOMMENDED DIMENSION
蓝白裸线(不接地)



APPLICABLE FPC RECOMMENDED DIMENSION
一体补强板铝箔FFC线

PIN NO.	DIM B	DIM E	DIM F	DIM G
60	29.50	34.05	35.00	32.55

6.0 INTERFACE SIGNAL TIMING SPECIFICATION

6.1 Signal Timing Parameters

< Table 10. Timing Table >

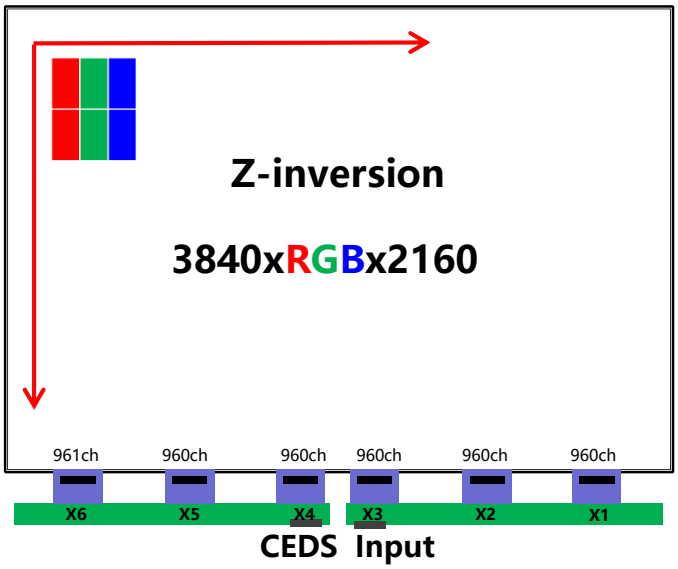
Item		Symbols	Min	Typ	Max	Unit
Frequency		1/Tc	69	74.25	78	MHz
Vertical	Frame Rate	F	57	60	62	Hz
	Total	T_V	2200	2250	2330	T_H
	Display	T_{VD}	2160			T_H
	Blank	T_{VB}	40	90	170	T_H
Horizontal	Total	T_H	530	550	570	T_{CLK}
	Display	T_{HD}	-	480	-	T_{CLK}
	Blank	T_{HB}	50	70	90	T_{CLK}

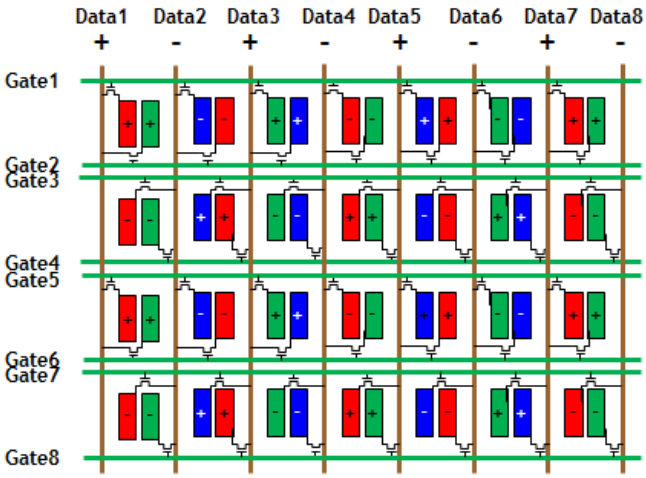
Item		Symbols	Min	Typ	Max	Unit
Frequency		1/Tc	69	74.25	78	MHz
Vertical	Frame Rate	F	47	50	51	Hz
	Total	T_V	2200	2700	2715	T_H
	Display	T_{VD}	2160			T_H
	Blank	T_{VB}	40	540	555	T_H
Horizontal	Total	T_H	530	550	570	T_{CLK}
	Display	T_{HD}	-	480	-	T_{CLK}
	Blank	T_{HB}	50	70	90	T_{CLK}

Notes:

1. This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.
2. This product should keep data frequency and Horizontal value fixed when adjusting frame rate.
3. This product supports frequency between 50Hz and 60Hz and Vertical & Horizontal values must follow the table.
4. This Timing specification is for LGE BM Maker.

6.2 Pixel Structure



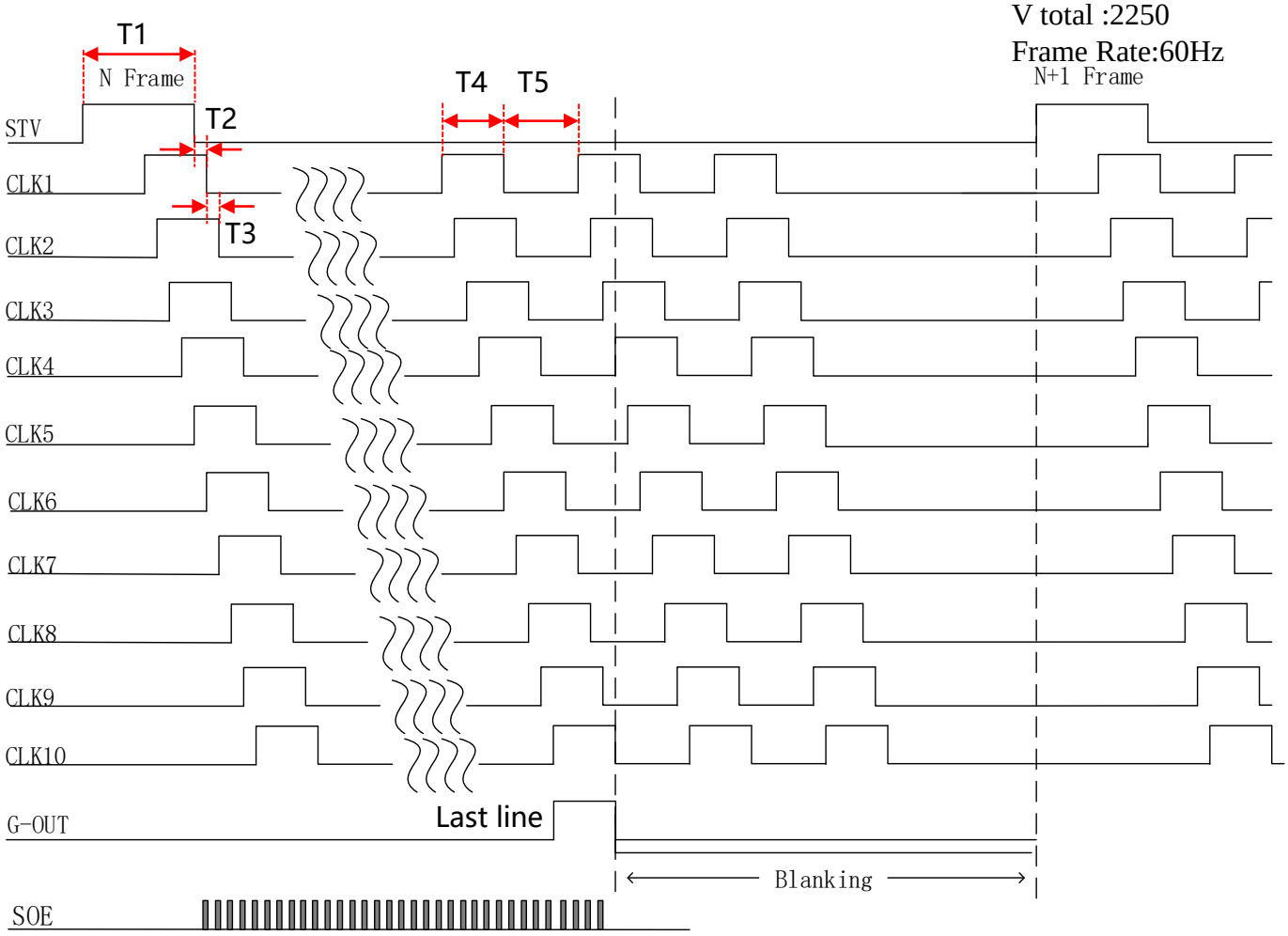


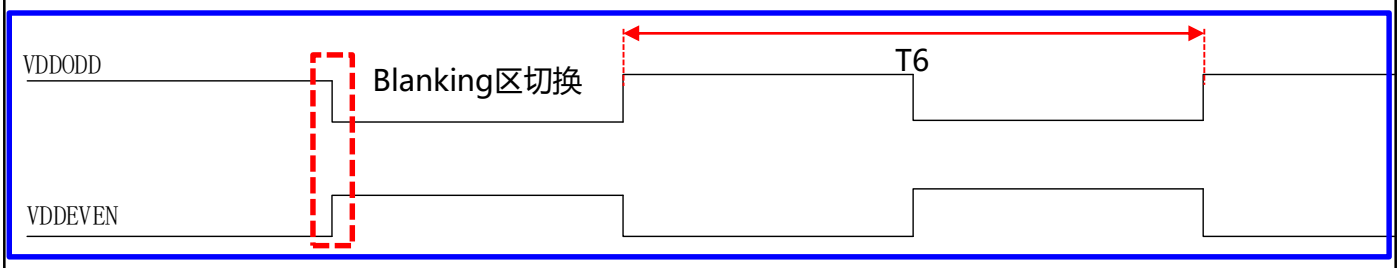
Notes:

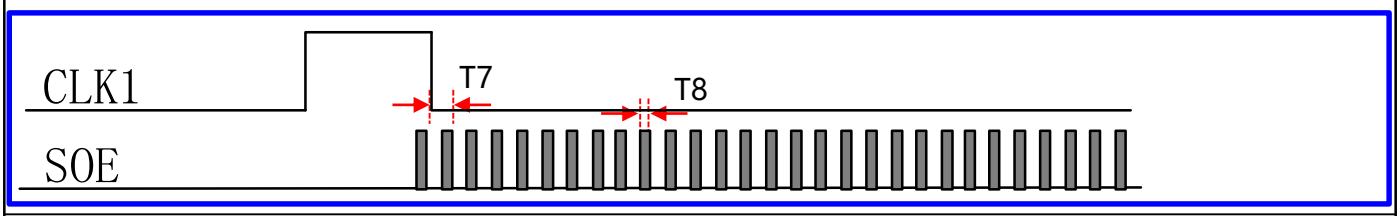
1. Panel is progressive scan from top to bottom.
2. Source driver data latch direction is from right to left.

6.3 Signal Timing Waveform

H total :4400
V total :2250
Frame Rate:60Hz







6.3 Signal Timing Waveform

H total :4400
V total :2250
Frame Rate:60Hz

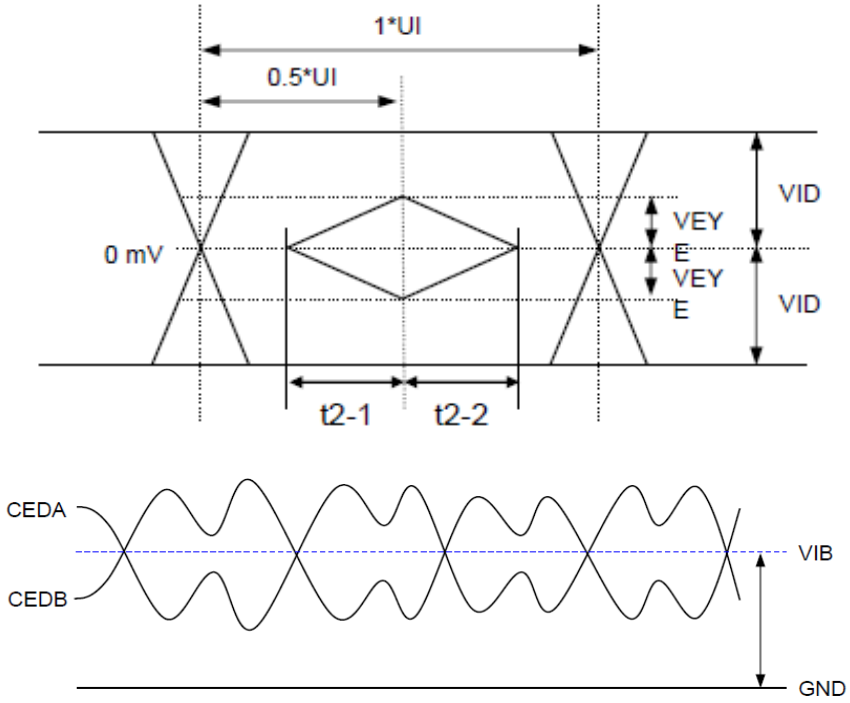
	Min.	Typ.	Max.	Description	Remark
T1	18.5us	25.9us	37us	STV Width(7H)	
T2	3.6us	3.7us	3.8us	CLK1 Falling to STV Falling（1H）	
T3	3.6us	3.7us	3.8us	CLK1 Falling to CLK2 Falling(1H)	
T4	13.8us	14.8us	15.8us	CLK High Width(4H)	
T5	21.2us	22.2us	23.2us	CLK Low Width(6H)	
T6	3s	4s	5s	VDDODD/VDDEVEN Period	Changed in blanking area
T7	1.9us	2.0us	2.1us	GOE	
T8	0.25us	0.38us	0.75us	SOE Width	

Notes:

1. 1H=1/（Frame Rate*V total）.
2. CLK2~CLK10 High Width is T4, same as CLK1.
3. CLK2~CLK10 Low Width is T5, same as CLK1.
4. CLK2 falling to CLK3 falling, CLK3 falling to CLK4 falling, CLK4 falling to CLK5 falling, CLK5 falling to CL K6 falling, CLK6 falling to CLK7 falling, CLK7 falling to CLK8 falling, CLK8 falling to CLK9 falling, CLK9 fal ling to CLK10 falling are all T3.
5. When power on, STV and CLK1~CLK10 should keep low before the first STV.
6. VDDODD and VDDEVEN must reverse in vertical blanking time.
7. Charging sharing function should be set up to by frame.

6.4 Signal Eye Diagram

< Table 11. CEDS Eye Diagram >



< Table 12. Eye Diagram information >

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Veye	VEYE	90	-	-	mV	
Eye-Open time	t2-1, t2-2	0.25	-	-	UI	
CEDS input differenctial voltage	VID	150	-	500	mV	
CEDS input common voltage	VIB	0.65	0.95	1.15	V	For LVDS Application
		0.65	VTERM-(VID/2)	-	V	For CML Application
	VTERM	1.08	1.2	1.32	V	

Notes :
1. Eye diagram test point is located on source board, close to source driver.
2. Driver IC screen condition: Vcm 0.6V, Veye 50mV, Data rate 3.4Gbps.
3. Measure condition: Normal temperature.

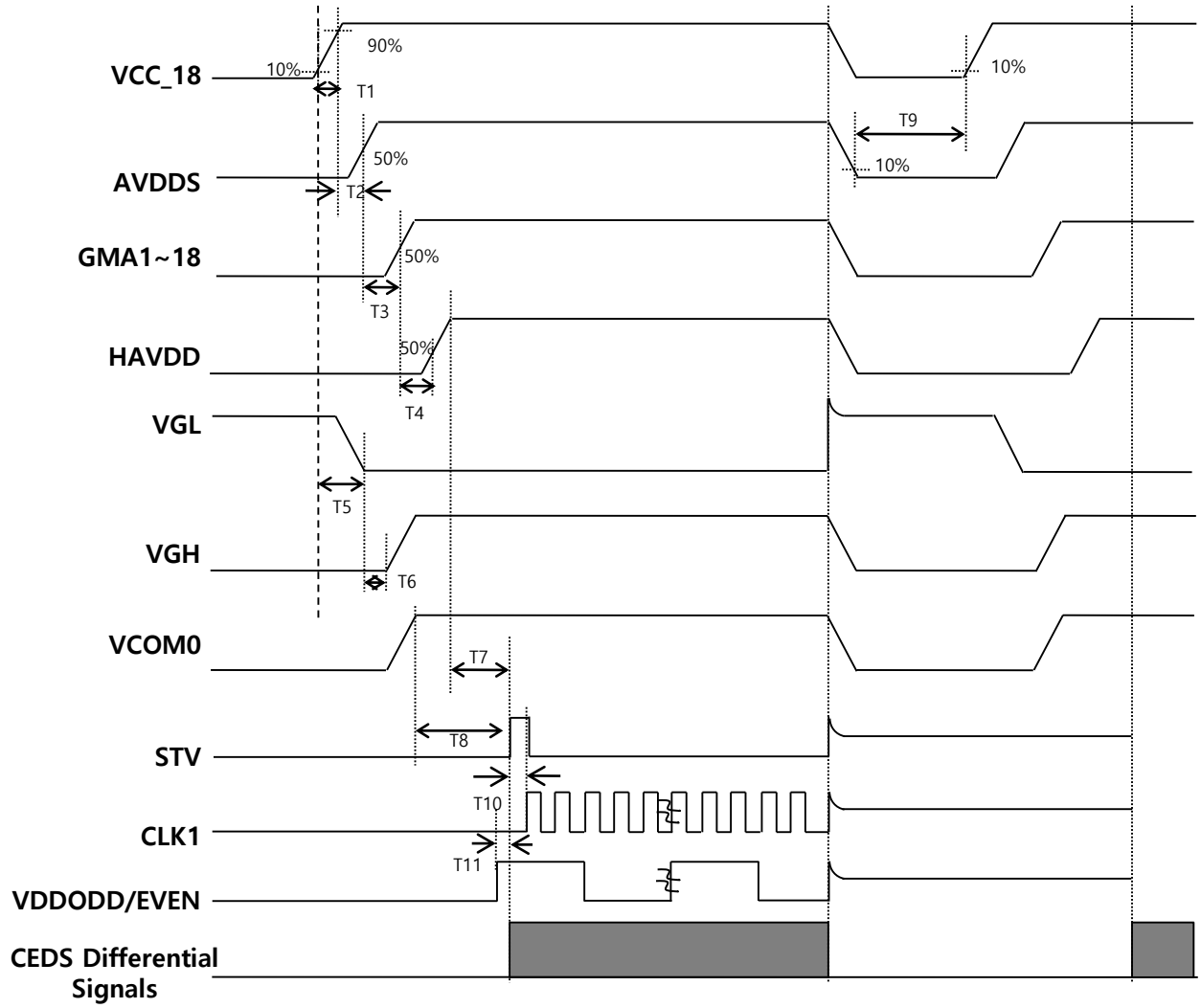
6.4 Signal Eye Diagram

< Table 13. Eye Diagram measurement conditions >

Oscilloscope PLL setting	
PLL type	2nd order PLL (=Type II PLL)
Bandwidth	5MHz
Damping Factor	700m
SSC	OFF
Real Time *	Applying (Disable DSP @Tektronix)
Accumulate UIs	Over than 1frame Data (≒27,000,000 Uis @UHD)

Notes :
1. Please use the measurement results just for your reference.
2. Eye measurement results using the Oscilloscope PLL are inaccurate because CEDS uses the DLL.

7.0 POWER SEQUENCE



Notes :

1. When power off, VGL,STV,CLK,VDDODD/VDDEVEN timing should follow VGH falling.
2. VGH is on SOC board only, so T6 time is tested on SOC board.
3. Gate CLK sequence is CLK1->CLK2->CLK3->CLK4->CLK5->CLK6->CLK7->CLK8->CLK9->CLK10.

7.0 POWER SEQUENCE

T	Min	Type	Max	Unit	Note
T1	0	-	10	ms	
T2	0	-	-	ms	
T3	0	-	-	ms	AVDDS must be higher than HAVDD and GMA all the time
T4	-200	-	1000	ms	AVDDS must be higher than HAVDD and GMA all the time
T5	0	-	-	ms	
T6	0	-	-	ms	
T7	0	-	-	ms	
T8	0	-	-	ms	
T9	1	-	-	s	
T10	13.8	14.8	15.8	us	STV to CLKs
T11	>2	-	-	Frame	VDD rising edge to First STV rising edge

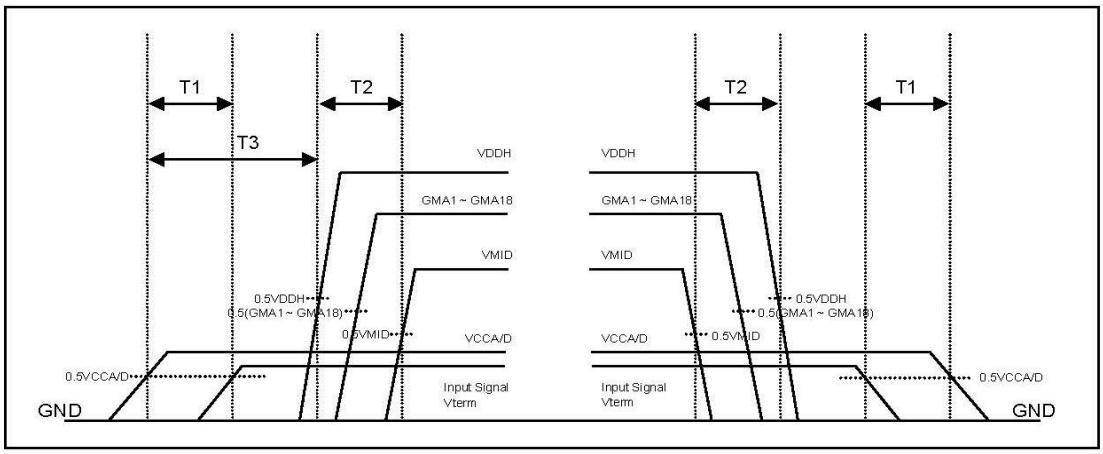
7.1 POWER SEQUENCE for Driver IC

- We guarantee below cases for the power sequence.

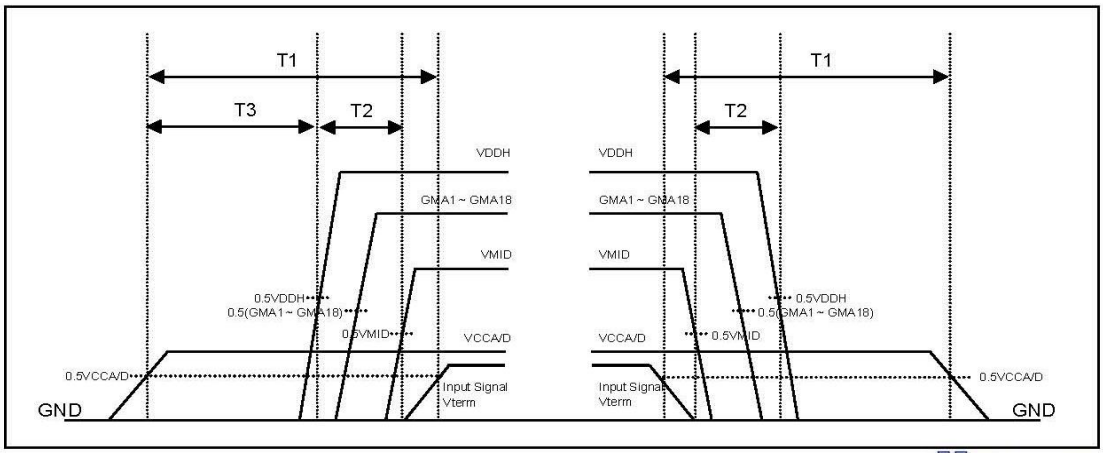
Parameter	Value			Units	Remarks
	Min.	Typ.	Max		
T1 1)	0	-	1000	ms	
T2 2)	-200	-	1000	ms	Always, VDDH must be Higher than or same with VMID and GMAx(x=1~18)
T3 3)	0	-	1000	ms	

Note. 1) time between VCC and input signal & Vterm
2) time between VDDH and GMAx & VMID
3) time between VCC and VDDH

1. Case1



2. Case2



8.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

< Table 14. Reliability Test Parameters >

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity storage test	Ta = 60 ℃, 90%RH, 240hrs
4	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240hrs
5	High temperature operation test	Ta = 50 ℃, 240hrs
6	Low temperature operation test	Ta = -5 ℃, 240hrs
7	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle

Note : Test condition is based on BOE module.

9.0 PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD Open Cell.

9.1 Precautions when taking out the Panel

- Pick the pouch only, when taking out panel from a shipping package.
- Recommend to use suitable sucker to pick up and put down panel.

9.2 Precautions for handling the panel

- As the electrostatic discharges may break the LCD panel, handle the LCD panel with care. Peel a protection sheet off from the LCD panel surface as slowly as possible. Refer to the appendix 4.
- As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD panel should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Put the panel display side down on a flat horizontal plane.
- Handle connectors and cables with care.

9.3 Precautions for the operation

- The LCD product shall be operated under normal conditions as below:
  - Temperature: 20±15℃
  - Humidity: 55±20%
  - Display pattern: continually changing pattern(Not stationary)
- Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions such as high temperature, high humidity, high altitude, special display patterns, long time operation, outdoor operation, etc.., it is strongly recommended to contact BOE for the advice about the application of engineering. Otherwise its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock markets, and controlling systems.
- Do not exceed the absolute maximum rating value.
- Periodical power-off or screen save is needed after long-term display. Product reliability and functions may not be guaranteed when it under 24 hours operation continuously per day.

9.0 PRECAUTIONS

- Do not insert or pull out the interface connector while the LCD panel is operating.
- LCD Response time depends on the temperature.(In lower temperature, it becomes longer)
- Ensure all input signals and power supplies are complete and valid when the panel is operating. Otherwise the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the panel would be damaged. Specially, pay attention to the turn on and off sequence.

9.4 Precautions for the atmosphere

- Storage atmosphere requirement.

ITEM	UNIT	MIN	MAX
Storage Temperature	(℃)	5	40
Storage Humidity	(%RH)	35	75
Storage Life	6 months		
Storage Condition	• The storage room should be equipped with a dark and good ventilation facility. • Prevent products from being exposed to the direct sunlight, moisture and water. • The product need to keep away from organic solvent and corrosive gas. • Be careful for condensation at sudden temperature change. • Storage condition is guaranteed under packing conditions.		

- Dew drop atmosphere should be avoided. When expose to drastic fluctuation of temperature (hot to cold or cold to hot), the LCD module may be affected. Specifically, drastic temperature fluctuation from cold to hot, produces dew on the LCD module's surface which may affect the operation of the polarizer and LCD module.
- Do not store and/or operate the LCD panel in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

9.5 Precautions for the panel characteristics

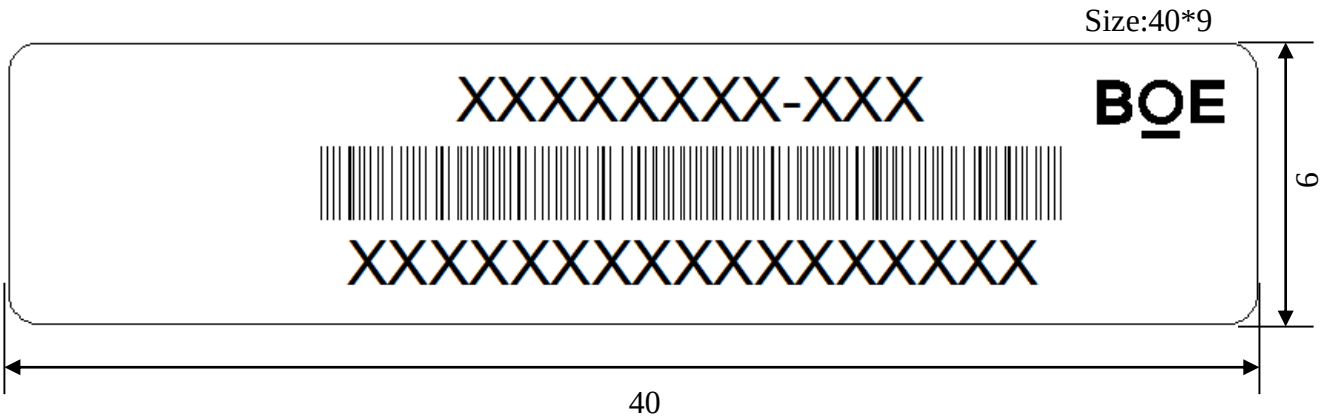
- Do not apply fixed pattern data signal to the LCD panel at product aging.
- Applying fixed pattern for a long time may cause image sticking.

9.0 PRECAUTIONS

9.6 Other precautions

- In particular in winter, Before putting Panel boxes on the line, aging process is required to make the temperature of products similar to the temperature of workplace.
- Do not disassemble and/or re-assemble LCD panel.
- Do not re-adjust variable resistor or switch etc.
- When returning the panel for repair or etc., Please pack the panel not to be broken. We recommend to use the original shipping packages.
- Product assembled into module should be stored in the bag(cover case).
- Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- Be careful not to give any extra mechanical stress to the panel when designing the set, and backlight.
- Do not pull, fold or bend the source COF and the gate COF in any processes.
- If the liquid crystal material leaks from the panel, this should be kept away from the eyes or mouth. If this contacts to hands, legs, or clothes, you must washed it away with soap thoroughly and see a doctor for the medical examination.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

10.0 PRODUCT SERIAL NUMBER



MDL ID Naming Rule:

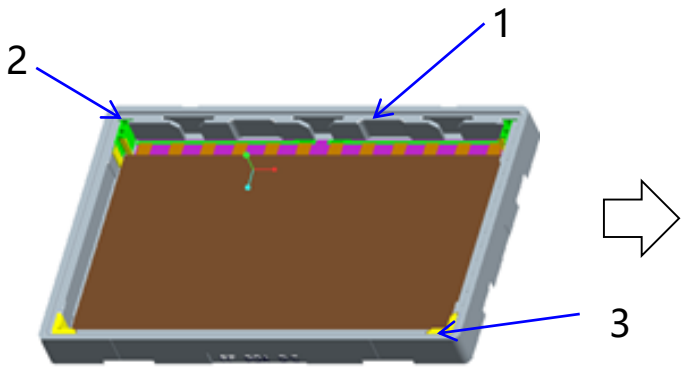
Digit / Code	1	2	3	4	5	6	7	8	9	10	11
Description	Model Code GBN		Grade	Line	Year		Month	Model Extension Code			
Digit / Code	12	13	14	15	16	17	18				
Description	Serial No						扫码不显示，BOE厂内用				

11.0 Packing

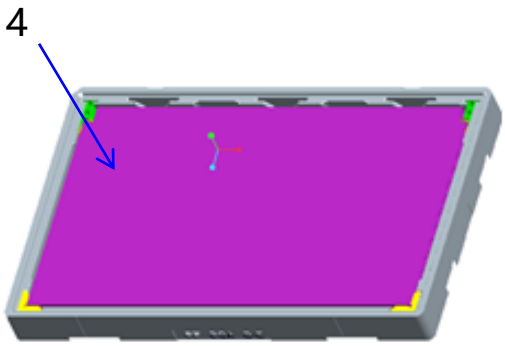
BOE provides the standard shipping container for customers, unless customer specifies their packing information. The standard packing method and Barcode information are shown in below.

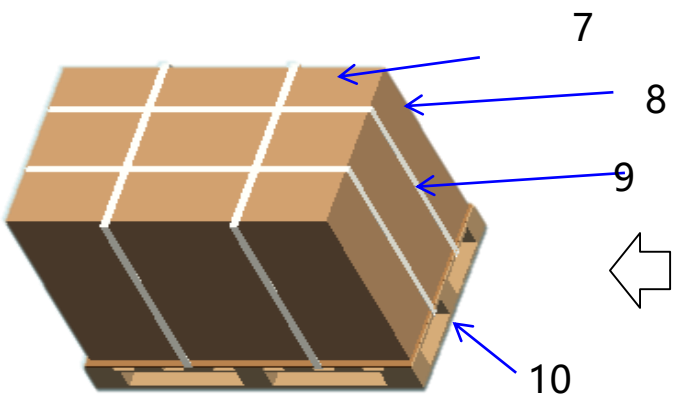
11.1 Packing Order

Put 1Pcs EPE Pad in the box, then put 1Pcs Panel into the box

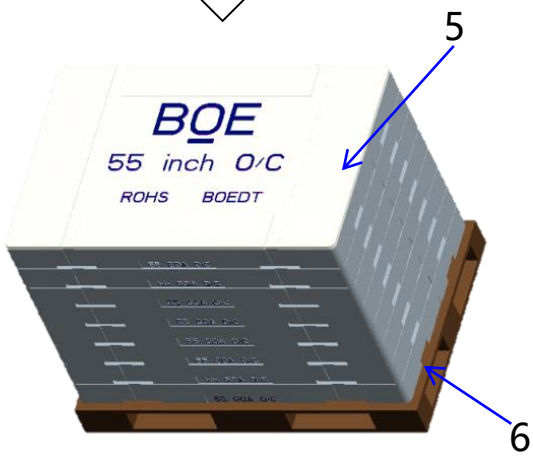


Totally 16pcs panels and 17Pcs EPE Pad per box





Place wrap film around the boxes.
Pack with 4 packing belts.



Put one paper pad on the pallet,
Put totally 8boxes and 1 cover.

N0.	Description	Material
1	Bottom	EPO
2	Cushion	ABS
3	Cushion	EPP
4	Spacer	EPE
5	Cover	EPO
6	Pad	Paper
7	Outbox	Paper
8	Film	PE
9	Band	PP
10	Pallet	Wood

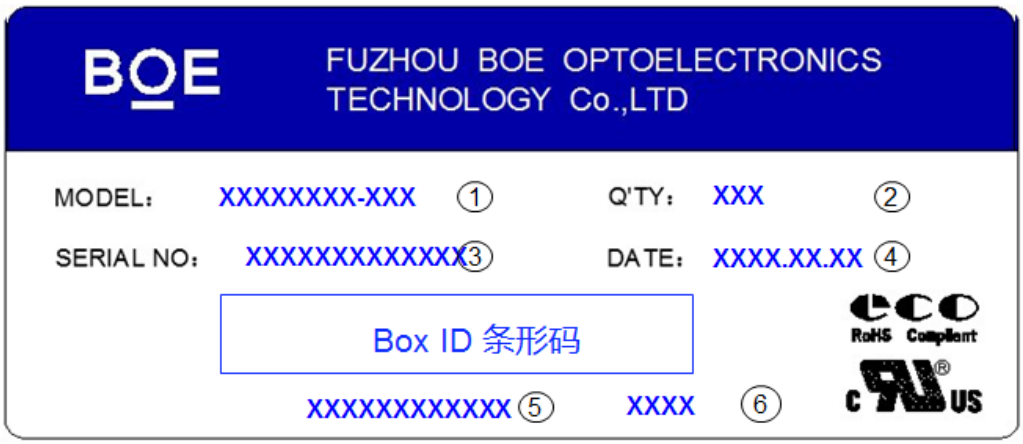
11.2 Packing Note

- Box Dimension : 1350mmL×868mmW×122mmH
- Package Quantity in one Box : 16pcs
- Wood Pallet Dimension : 1380mmL x 900mmW x130mmH

11.3 Box Label

- Label Size : 70 mm (L) × 30 mm (W)
- Contents

  Model : HV550QUB-F1D
  Q`ty : 16 Open Cell in one box
  Serial No. : Box Serial No.
  Date : Packing Date



打印内容，说明如下:

① FG-CODE
② 产品数量
③ Box ID, 编码规则如下
④ Box Packing 日期
⑤ 产品物料号(客户端)
⑥ FG-CODE 后四位

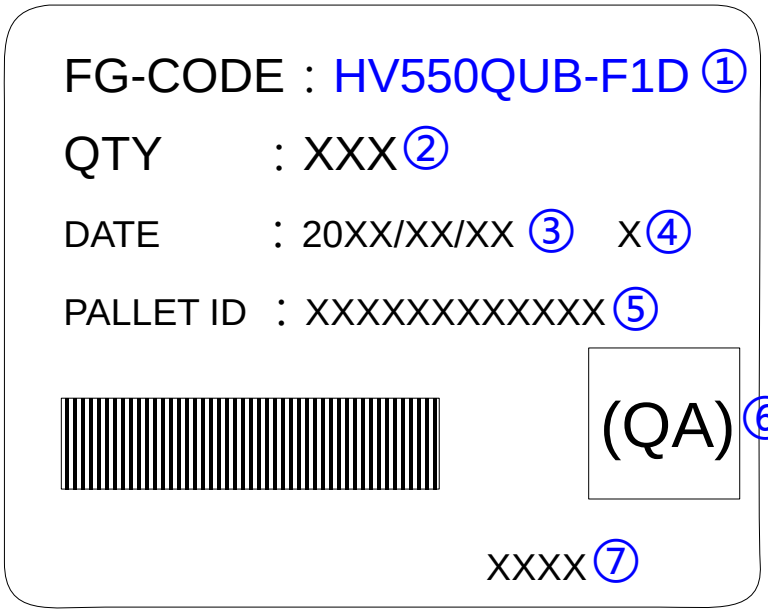
Box ID Naming Rule:

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	X	X	X	X	1	6	3	D	0	0	1	A	1
Description	Products GBN		Grade	Line	Year		Month	Revision Code	Serial No.				

11.4 Pallet Label

- Label Size : 100 mm (L) × 80 mm (W)
- Contents

  Model : HV550QUB-F1D
  Q`ty : Open Cell quantity in one pallet.
  Pallet ID: Pallet ID See next for detail description.
  Date : Packing Date

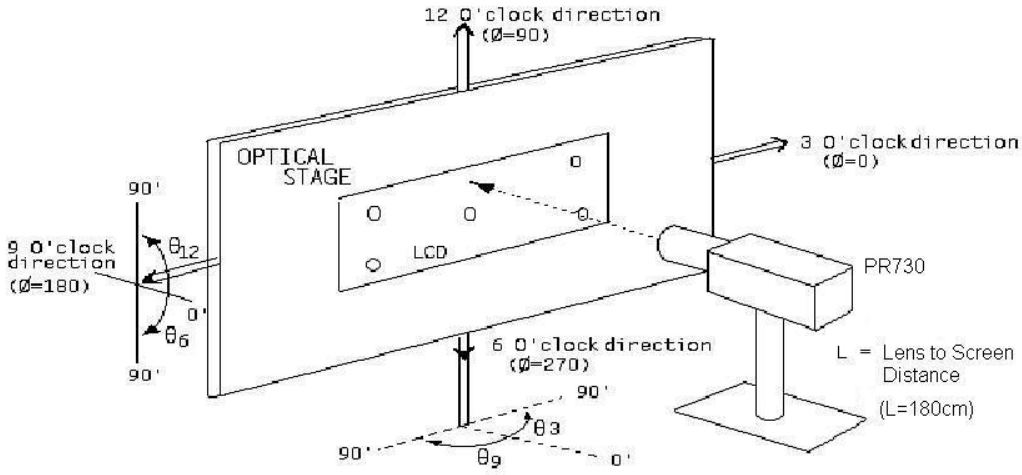


1. FG-CODE(The first twelve number)
2. Open Cell quantity in one pallet
3. Pallet Packing Date
4. E:Export D:Domain
5. Pallet ID
6. QA Mark
7. FG-CODE(The last four number)

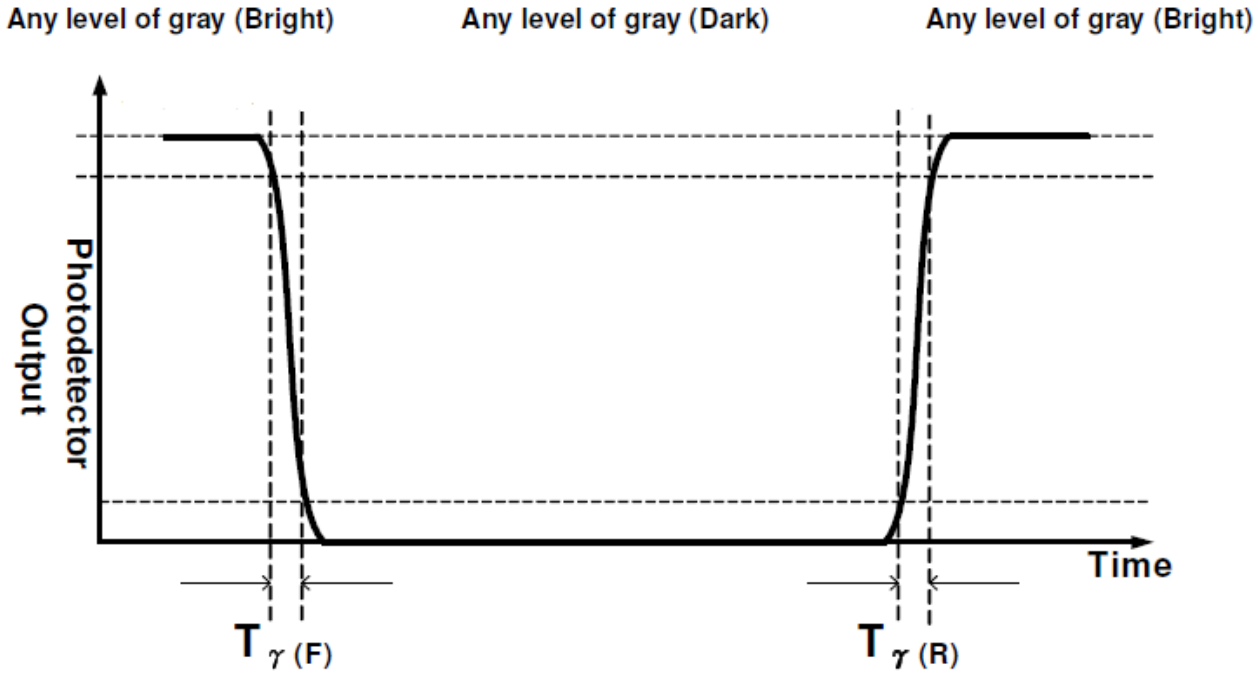
Pallet ID Naming Rule:

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12
Code	2	0	1	9	3	N	M	0	0	5	6	7
Description	Year				Month	Line	Pallet 方式	Serial No				

12.0 APPENDIX 1

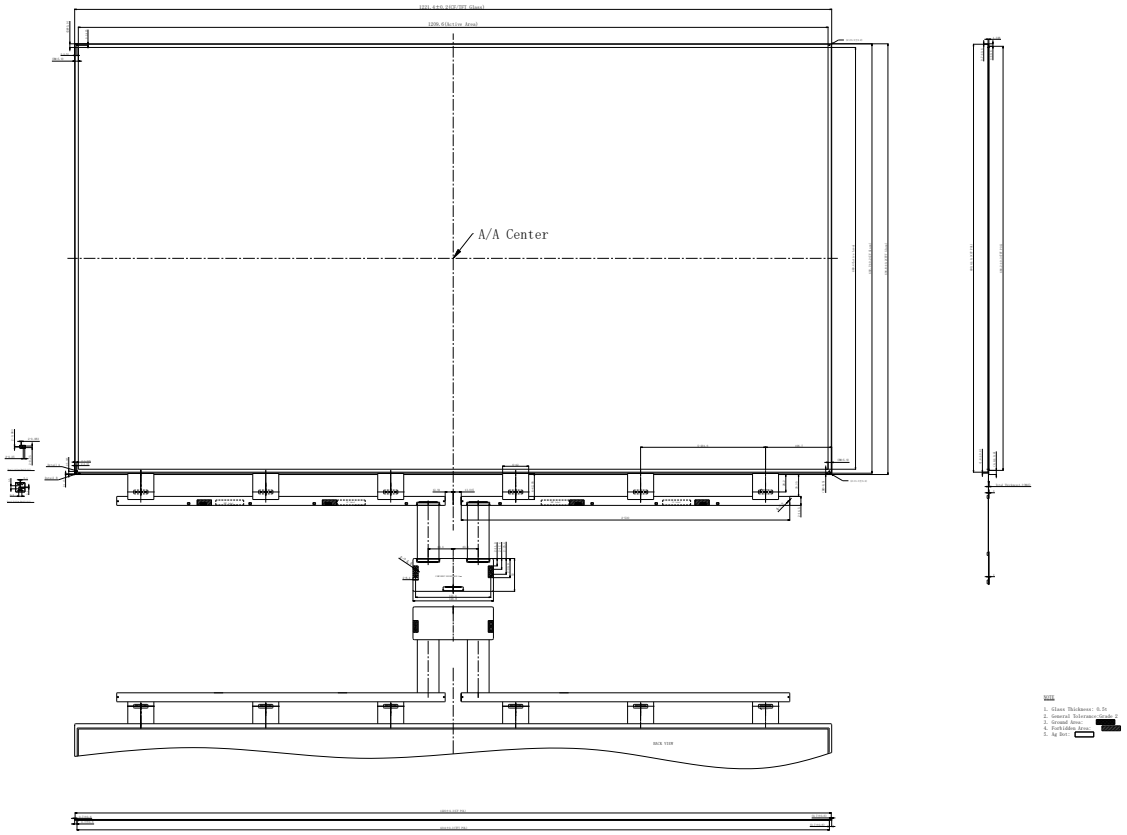


< Figure 1. Measurement Set Up >



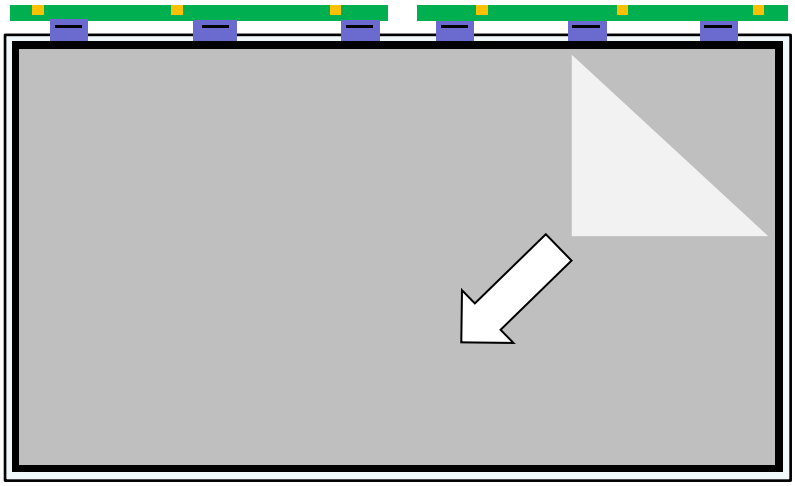
< Figure 2. Response Time Testing >

12.0 APPENDIX 2



< Figure 3. TFT-LCD Open Cell Outline Dimensions (Front View) >

12.0 APPENDIX 3



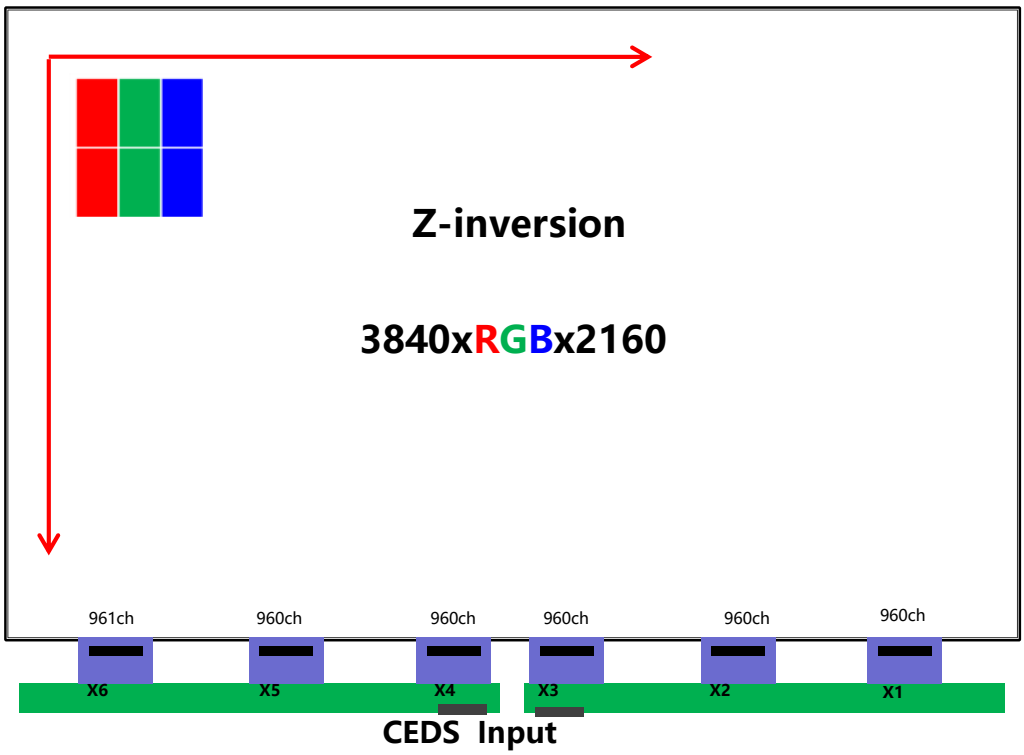
< Figure 4. TFT POL Protect Film Peeling Method >

Peeling Step:

1. Be sure to peel off slowly(recommended more than 7sec) and constant speed.
2. Peeling direction shows in Figure 4.
3. Be sure to ground person with adequate methods such as the anti-static wrist band.
4. Be sure to ground each source PCB while peeling off the protection film.
5. Ionized air should be blown over during peeling action.
6. The protection film must not touch drivers and source PCBs.
7. If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.

12.0 APPENDIX 4

This product is reverse type display. RGB data mapping scan direction : from left-up to right-down.



< Figure 5. Display Mode>

12.0 APPENDIX 5

< Table 1. EQ Profile>

EQ Option	DC gain(V/V)	Zero (GHz)	Pole1(GHz)	Pole2(GHz)
LL	1.0	1.0	1.45	3.2
LH	1.0	0.7	1.45	3.2
HL	1.0	0.5	1.32	3.2
HH	1.0	0.35	1.28	3.2

< Table 2. SSC Modulation>

SSC modulation frequency	SSC modulation ratio (%)
~50KHz	+/- 2.0%
60KHz	+/- 1.8%
70KHz	+/- 1.6%
80KHz	+/- 1.4%
90KHz	+/- 1.2%
100KHz	+/- 1.0%

※ Note :
SW98123A SSC modulation ratio Formula (modulation freq.=50KHz~100KHz)
Modulation ratio = 3 – 0.02*Fmod (Fmod unit is KHz)

12.0 APPENDIX 6

International Standards

1. Environment

a) RoHS, Commission Delegated Directive (EU) 2015/863 of 31 March 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council

b) REACH, Regulation (EC) No 1907/2006 of the European Parliament and of the Council of 18 December 2006 concerning the Registration, Evaluation, Authorization and Restriction of Chemicals