

Model name: PT650GT01-4

Date: 03. Nov. 2022

(☒) Preliminary Specification

(☐) Final Specification

Any modification is not allowed without HKC's permission

Customer's Approval	Changsha HKC
Approved by	Approved By Product Director Date
Company(公司): _____	Name: _____ Signature: _____
Title(职称): _____	Reviewed By PM Manager Date
Signature(签名): _____	Name: _____ Signature: _____
Note	Reviewed By Project Leader Date
	Name: _____ Signature: _____
	Reviewed By PM Date
	Name: _____ Signature: _____

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Revision History

Version	Date	Page (New)	Section	Description	Revision by
Rev. P1	2022/11/03	-	All	Preliminary Specification was first issued.	RD

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1. GENERAL DESCRIPTION

The specification is applied to 65" model (PT650GT01-4) TFT Liquid Crystal Display open cell and it supports 3840x2160 UD mode with 1.07G colors (8bit+FRC). This product is with driver ICs and a 51-pins-8 lane-VBO circuit board and built in without backlight unit.

1.1 General Specifications

Item	Specification	Unit	Note
Screen Size	65 inch Diagonal	-	-
Outline Dimension	1440.48(H) × 816.02(V) × 1.361(D)	mm	-
Active Area	1428.48(H) × 803.52(V)	mm	-
Driver Element	a-Si TFT active matrix	-	-
Cell Transmittance	5.5(Typ.)	%	HKC light , center point
Pixel Number	3840 × 2160	pixel	-
Sub Pixel Pitch	0.124 (H) × 0.372 (V)	mm	-
Pixel Arrangement	1 Flip/RGB vertical	-	-
Display Colors	1.07G	color	8bit+FRC
Display Mode	Normally Black	-	-
Display Orientation	Signal input with "ABC"	-	-
Panel Inversion Type	Column inversion	-	-
Surface Treatment	Type=AG	-	-
	Haze=3%	-	-
	Top surface Hardness:3H	-	-
Weight	3.31	Kg	-

Note:

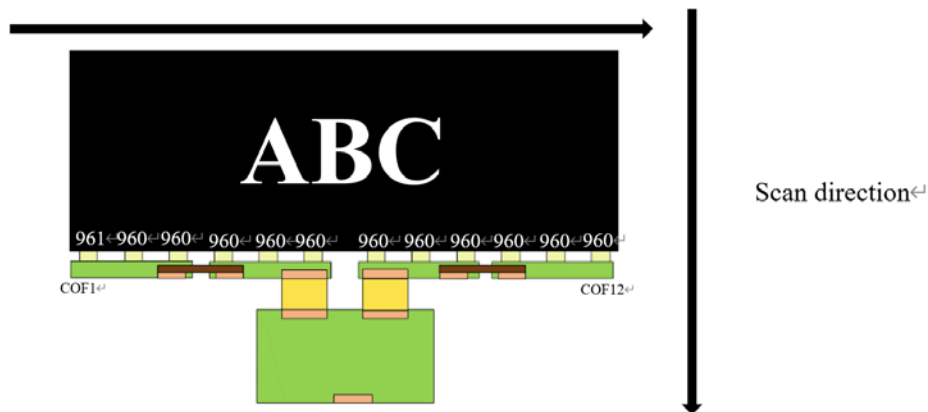


Fig 1.1 Display Orientation

2. ABSOLUTE MAXIMUM RATINGS

2.1 Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Input Signal Voltage	V_{in}	-0.3	3.6	V	(1)

Note:

- (1) Within $T_a=25\pm2^{\circ}\text{C}$
- (2) a. 90 % RH Max. ($T_a \leq 40^{\circ}\text{C}$)
 - b. Web-bulb temperature should be 39°C Max. ($T_a > 40^{\circ}\text{C}$)
 - c. No condensation
 - d. Operating condition with a assemble module.
- (3) The temperature of panel surface should be 0°C min. and 50°C max.
- (4) Any point on the Driver surface must be less than 120°C under any condition. Module designer should apply adequate thermal solutions to keep the electrical components surface temperature under control limit (ex: Source Driver IC 120°C , Components on T-con PCB 100°C). Operation over the temperature can cause damages or decrease of life time.

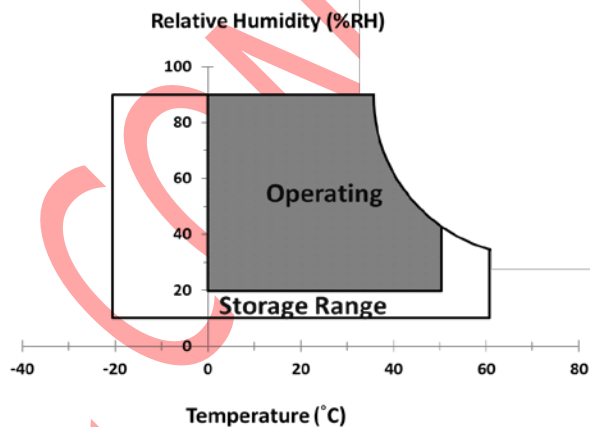


Fig. 2.1 Operating and storage environment

3. ELECTRICAL SPECIFICATIONS

3.1 Electrical Characteristics

3.1.1 Power Consumption

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	5	A	(2)
Power Supply Current	White Pattern	-	-	0.524	0.685	A	(3)
	Horizontal Strip	-	-	1.61	2.093	A	
	Black Pattern	-	-	0.482	0.626	A	
Power Consumption	White Pattern	P_e	-	6.28	8.16	W	
	Horizontal Strip		-	19.32	25.11	W	
	Black Pattern		-	5.78	7.78	W	

Note:

- (1) Ambient temperature: $25 \pm 2^\circ\text{C}$
- (2) The ripple voltage should be controlled under 10% of V_{CC} .
- (3) Measurement Conditions: V_{CC} rising time = $470\mu\text{s}$.

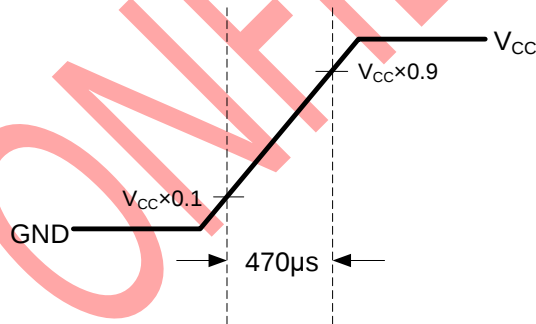


Fig.3.1 V_{CC} rising time condition

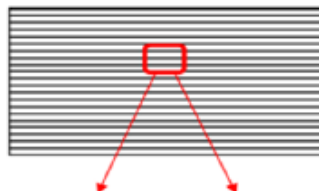
- (1) Measurement Conditions: $V_{CC} = 12\text{V}$, $T_a = 25 \pm 2^\circ\text{C}$, $F_v = 60\text{ Hz}$, whereas the test pattern is shown as below.

The heavy load pattern is figure B.

A. White Pattern



B. Horizontal Strip



C. Black Pattern



Fig.3.2 Test patterns

3.1.2 V By One Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
V by one Interface	Differential Input High Threshold Voltage	VTH	-	-	+50	mV	-
	Differential Input Low Threshold Voltage	VTL	- 50	-	-	mV	-
	Intra-pair Skew	TTOSK_intra	-0.3	-	0.3	UI	(1)
	Inter-pair Skew	TTOSK_inter	-5	-	5	UI	(2)
	Spread Spectrum Modulation range	30KHz modulation	-0.5	-	+0.5	%	(3)(4)
	Spread Spectrum Modulation frequency	FSSM	-	-	30K	Hz	
	Differential Input Swing Voltage	V	200	-	400	mV	-
CMOS Interface	Input High Threshold Voltage	VIH	2.4	-	3.3	V	-
	Input Low Threshold Voltage	VIL	0	-	0.6	V	-
Data rate		-	-	2.97	-	-	Gbps
Loop bandwidth		-	-	10	-	-	MHZ
Damping factor		-	-	1	-	-	-

Note:

(1) Intra-pair skew

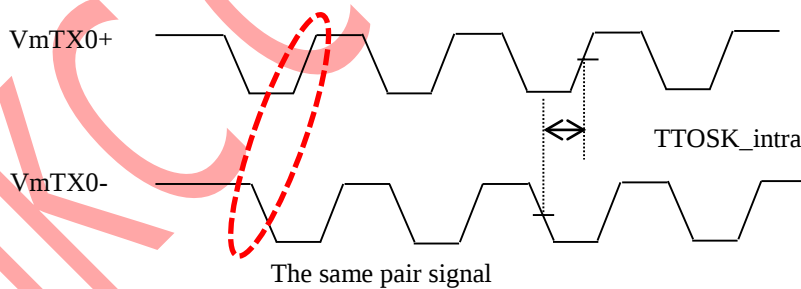


Fig. 3.3 V by one Intra-pair skew

(2) Inter-pair skew

Lane0: $V_{diff} = (V_{mTX0+}) - (V_{mTX0-})$

Lane1: $V_{diff} = (V_{mTX1+}) - (V_{mTX1-})$

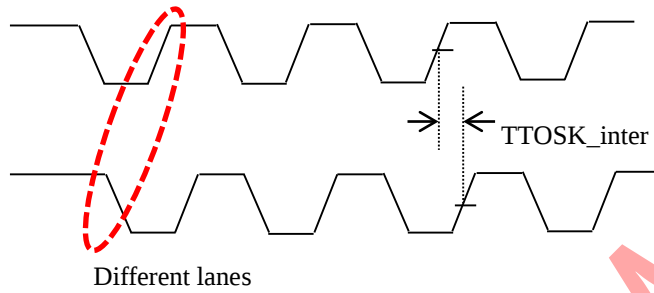


Fig. 3.4 V by one Inter-pair skew

(3) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure.

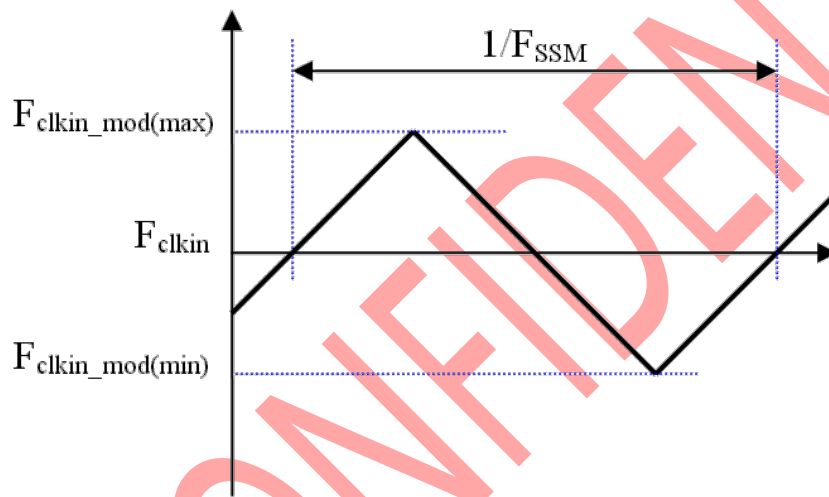


Fig. 3.5 Spread Spectrum Clock Generator

(4) The V by one SSM's suggestion is off by default, SOC board must test all validation if SOC board open the V by one SSM.

Item	X(UI)	Y(mV)	Note
A	0.25	0	(1)
B	0.3	50	(1)
C	0.7	50	(1)
D	0.75	0	(1)
E	0.7	-50	(1)
F	0.3	-50	(1)

The diagram illustrates the timing characteristics of a 64QAM signal. The top portion shows the signal waveform, which is a complex periodic signal. The bottom portion shows the eye diagram, which is a plot of the signal's amplitude over time. The eye diagram is divided into two main regions by vertical dashed lines labeled $X=0$ UI and $X=1$ UI. The horizontal axis is labeled t_{RBIT} (bit period). The vertical axis is labeled $Y-0$ mV. The eye diagram shows the signal's amplitude over time, with the signal's amplitude varying between approximately ± 1.5 mV. The eye diagram is divided into two main regions by vertical dashed lines labeled $X=0$ UI and $X=1$ UI. The horizontal axis is labeled t_{RBIT} (bit period). The vertical axis is labeled $Y-0$ mV. The eye diagram shows the signal's amplitude over time, with the signal's amplitude varying between approximately ± 1.5 mV. The eye diagram is divided into two main regions by vertical dashed lines labeled $X=0$ UI and $X=1$ UI. The horizontal axis is labeled t_{RBIT} (bit period). The vertical axis is labeled $Y-0$ mV. The eye diagram shows the signal's amplitude over time, with the signal's amplitude varying between approximately ± 1.5 mV.

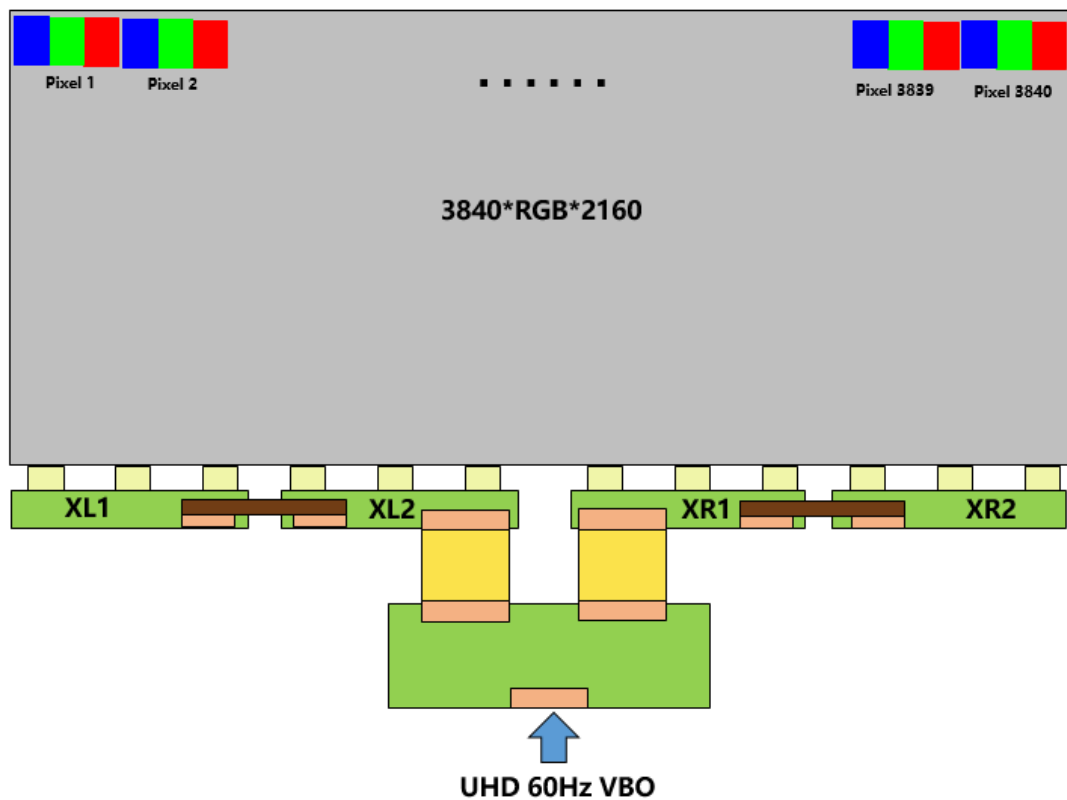
Fig. 3.6 V by one input signal timing

3.1.4 V By One Data Mapping

V by One Data Mapping

Lane	Data Stream
Lane 0	Pixel 1, 5, 9,,1913, 1917
Lane 1	Pixel 2, 6, 10,,1914, 1918
Lane 2	Pixel 3, 7, 11,,1915, 1919
Lane 3	Pixel 4, 8, 12,,1916, 1920
Lane 4	Pixel 1921, 1925, 1929,,3833, 3837
Lane 5	Pixel 1922, 1926, 1930,,3834, 3838
Lane 6	Pixel 1923, 1927, 1931,,3835, 3839
Lane 7	Pixel 1924, 1928, 1932,,3836, 3840

TFT LCD Panel



3.1.5 Color Data Input Assignment

The brightness of each primary color is based on the 10-bit gray scale data input for each color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus.

Data Input Color		Data Signal																																							
		Red										Green										Blue																			
		MSB										LSB										MSB										LSB									
R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0												
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0										
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1										
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1										
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1										
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0										
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1										
Gray Scale of Red	Red (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
	Red (001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
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	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
Gray Scale of Green	Green (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
	Green (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0										
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	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0										
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0										
Gray Scale of Blue	Blue (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
	Blue (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1										
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	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0										
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1										

Attention:

0: Low level voltage; 1: High level voltage.

3.2 Interface Connections

Interface Pin Assignment

CN1: F05035-51P-U (CT) or equivalent (1)

Pin No.	Symbol	Description	Pin No.
1	VIN12	Power input (+12V)	-
2	VIN12	Power input (+12V)	-
3	VIN12	Power input (+12V)	-
4	VIN12	Power input (+12V)	-
5	VIN12	Power input (+12V)	-
6	VIN12	Power input (+12V)	-
7	VIN12	Power input (+12V)	-
8	VIN12	Power input (+12V)	-
9	NC	No Connection	(2)
10	GND	Ground	-
11	GND	Ground	-
12	GND	Ground	-
13	GND	Ground	-
14	GND	Ground	-
15	SECTION	High(3.3V) for Two Section Open/Low(GND) for One Section	-
16	NC	No Connection	(2)
17	NC	No Connection	(2)
18	SDA	I2C Serial Data	-
19	SCL	I2C Serial Clock	
20	WP	Write Protection High(3.3V) for Writable, Open/Low(GND) for Protection	
21	BIST_MODE	BIST_EN H: Aging/L: Aging off BIST_SEL H: rotate pattern/L: black pattern	-
22	NC	No Connection	(2)
23	NC	No Connection	(2)
24	NC	No Connection	(2)
25	HTPDN	Hot Plug Detect	-
26	LOCKN	Lock Detect	-
27	GND	Ground	-
28	VB1_Rx0N	V-By One HS Negative Data Lane 0	-
29	VB1_Rx0P	V-By One HS Positive Data Lane 0	-

30	GND	Ground	-
31	VB1_Rx1N	V-By One HS Negative Data Lane 1	-
32	VB1_Rx1P	V-By One HS Positive Data Lane 1	-
33	GND	Ground	-
34	VB1_Rx2N	V-By One HS Negative Data Lane 2	-
35	VB1_Rx2P	V-By One HS Positive Data Lane 2	-
36	GND	Ground	-
37	VB1_Rx3N	V-By One HS Negative Data Lane 3	-
38	VB1_Rx3P	V-By One HS Positive Data Lane 3	-
39	GND	Ground	-
40	VB1_Rx4N	V-By One HS Negative Data Lane 4	-
41	VB1_Rx4P	V-By One HS Positive Data Lane 4	-
42	GND	Ground	-
43	VB1_Rx5N	V-By One HS Negative Data Lane 5	-
44	VB1_Rx5P	V-By One HS Positive Data Lane 5	-
45	GND	Ground	-
46	VB1_Rx6N	V-By One HS Negative Data Lane 6	-
47	VB1_Rx6P	V-By One HS Positive Data Lane 6	-
48	GND	Ground	-
49	VB1_Rx7N	V-By One HS Negative Data Lane 7	-
50	VB1_Rx7P	V-By One HS Positive Data Lane 7	-
51	GND	Ground	-

Note:

(1) direction of pin assignment is shown as below:

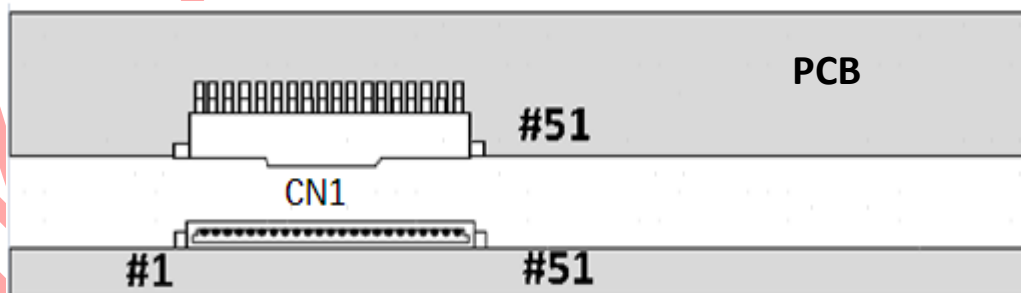
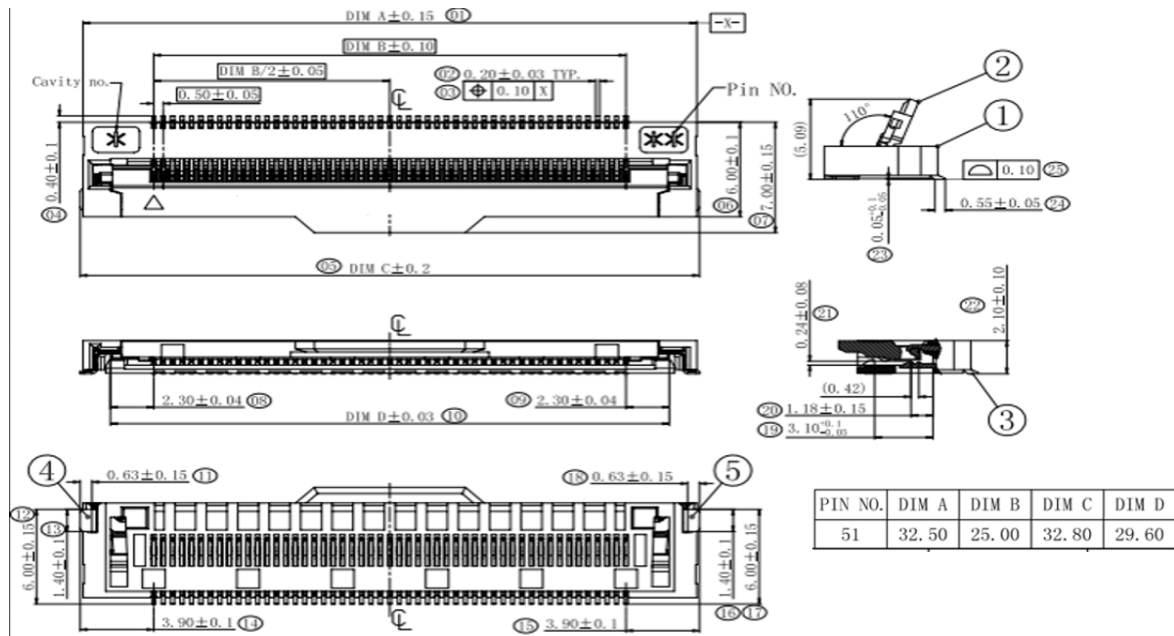


Fig 3.7 Connector direction sketch map

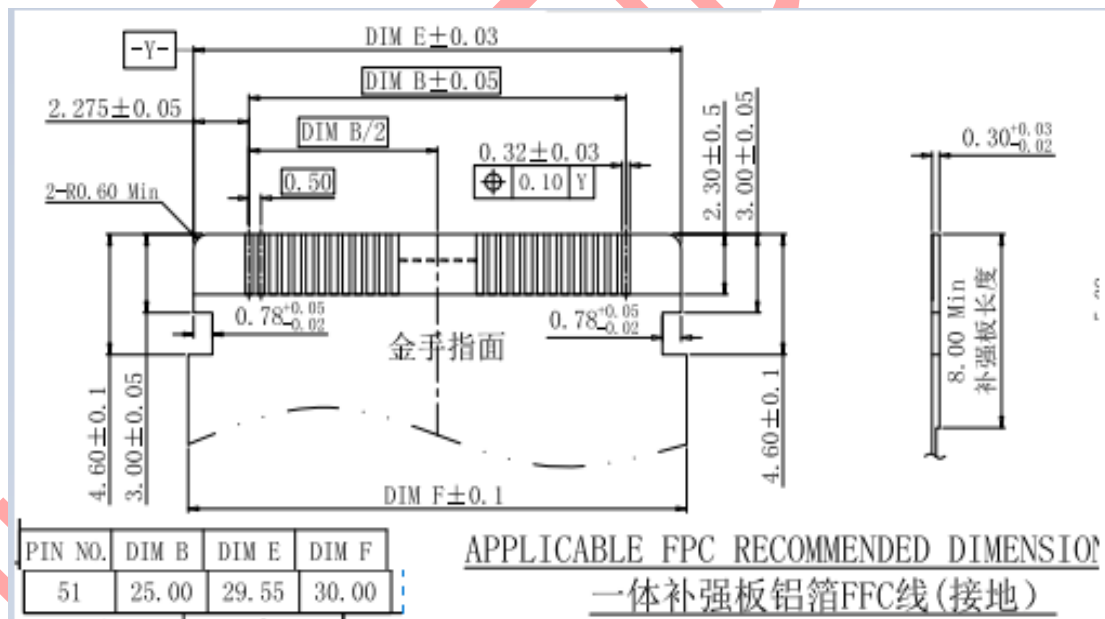
(2) Reserved internal use. Please leave it open.

(4) Connector Drawing

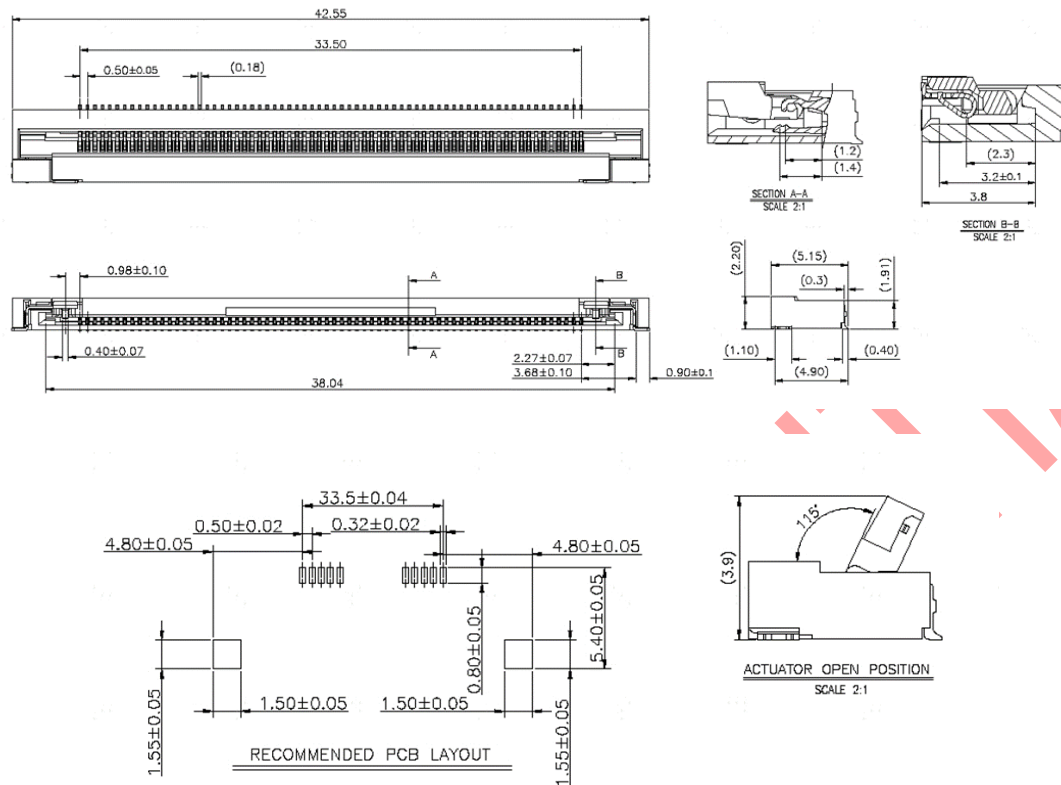
TCON Board Input 51pin Connector Drawing- F05035-51P-U



TCON Board Input 51pin FFC Drawing

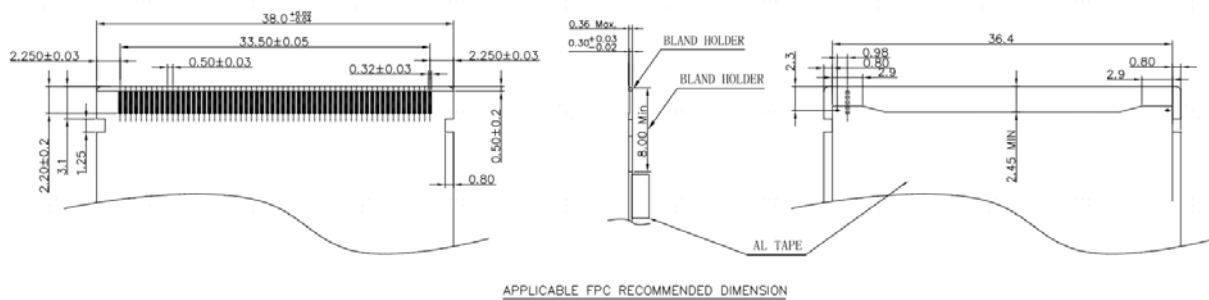


TCON Board Output 68 pin Connector Drawing- CAAHR068A



TCON Board Output 68pin FFC Drawing

FFC differential resistance $R_L=100\Omega\pm10\%$



3.3 IC Characteristics

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
TCON Surface Temperature	T _{TS}	-	-	110	°C
Driver Surface Temperature	T _{DS}	-	-	120	°C
PMIC Surface Temperature	T _{PS}	-	-	100	°C

Note :

- (1) Any point on the IC surface must be less than the max value under any conditions.
- (2) This test condition is based on HKC module

3.4 Timing Spec

Timing Table (DE Only Mode)

Frame Rate=60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frequency		F _{CLK} (= 1 / T _{CLK})	60	74.25	78.5	MHz	(1)
Frame Rate		F	58	60	62	Hz	-
Vertical Term	Total	T _V	2208	2250	2450	T _H	T _V = T _{VD} + T _{VB}
	Display	T _{VD}	2160			T _H	-
	Blank	T _{VB}	48	90	290	T _H	-
Horizontal Term	Total	T _H	530	550	600	T _{CLK}	T _H = T _{HD} + T _{HB}
	Display	T _{HD}	480			T _{CLK}	-
	Blank	T _{HB}	50	70	120	T _{CLK}	-

Frame Rate=50Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frequency		F _{CLK} (= 1 / T _{CLK})	60	74.25	78.5	MHz	(1)
Frame Rate		F	48	50	52	Hz	-
Vertical Term	Total	T _V	2208	2700	2800	T _H	T _V = T _{VD} + T _{VB}
	Display	T _{VD}	2160			T _H	-
	Blank	T _{VB}	48	540	640	T _H	-
Horizontal Term	Total	T _H	530	550	600	T _{CLK}	T _H = T _{HD} + T _{HB}
	Display	T _{HD}	480			T _{CLK}	-
	Blank	T _{HB}	50	70	120	T _{CLK}	-

Attention:

The module is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.

Note:

- (1) Please make sure the range of pixel clock follows the following equations:

$$F_{clk}(max) \geq F_{max} \times T_v \times T_h$$

$$F_{min} \times T_v \times T_h \geq F_{clk}(min)$$

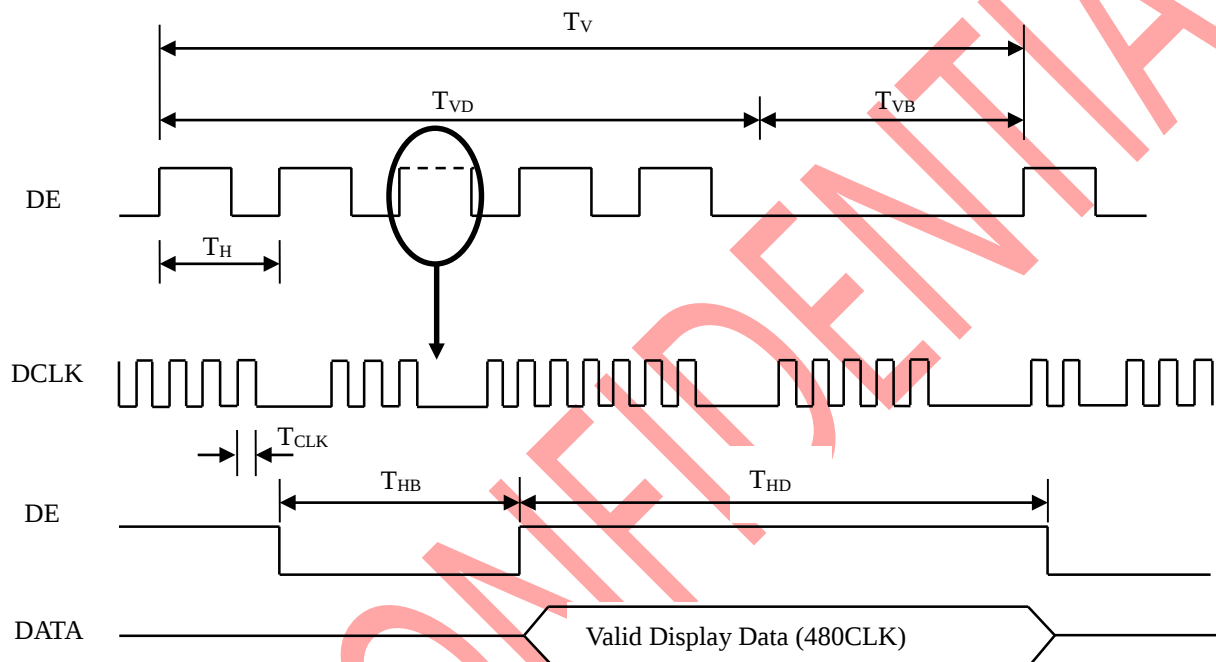


Fig.3.11 Interface signal timing diagram

3.5 Power On/Off Sequence

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.

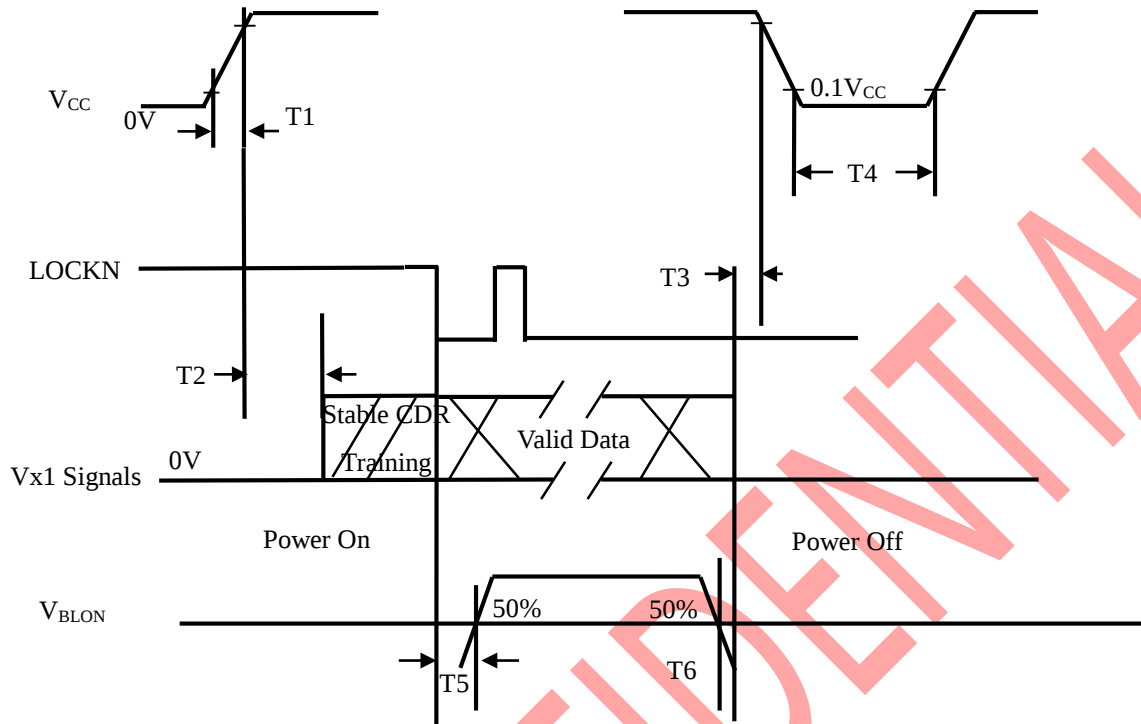


Fig. 3.12 Power on/off sequence

Parameter	Values			Unit
	Min.	Typ.	Max.	
T1	0.5			ms
T2	0			ms
T3	0			ms
T4	1000			ms
T5	500			ms
T6	100			ms

Attention:

- (1) Apply the light bar voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (2) In case that V_{CC} is in off level, please keep the level of input signals on the low or high impedance.
- (3) T4 should be measured after the module has been fully discharged between power off and on period.
- (4) Interface signal shall not be kept at high impedance when the power is on.
- (5) The product should be always operated within above ranges.

3.6 Flicker Pattern

The Flicker adjustment pattern suggested as below.



Bright sub-pixel=G127(50% grayscale); dark sub-pixel=G0 (0%grayscale)

Fig 3.13 Flicker pattern

3.7 Driver IC ESD spec

If the LCD module is designed with the Plastic Bezel, we suggest ESD protection solutions should be applied to avoid IC damaged, as shown in Fig.3.14.

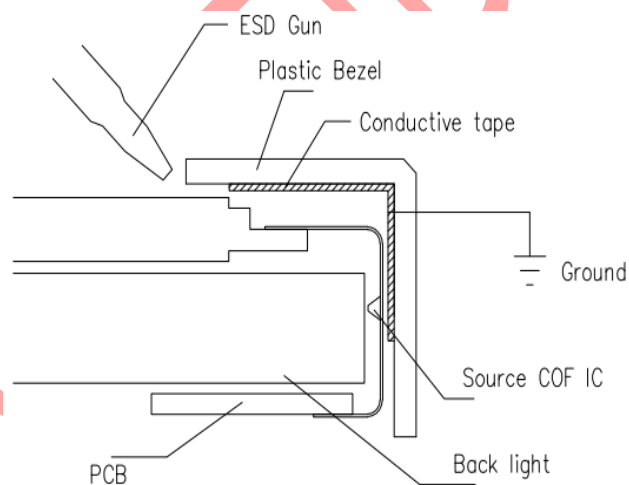


Fig. 3.14 Source COF IC ESD protection

4. OPTICAL CHARACTERISTICS

4.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25 ± 2	$^{\circ}\text{C}$
Ambient Humidity	H_A	50 ± 10	% RH
Supply Voltage	V_{CC}	12	V
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Vertical Refresh Rate	F_v	60	Hz
Light source	HKC module White LED Backlight Module/ Film structure		
Warm up time	T_{warm}	$>30 \text{ min}$	min
Dark room	ED	$1\text{lux}>$	lux

To avoid abrupt temperature change during optical measurement, the measurement should be executed in a stable, windless, in dark room after lighting the light source.

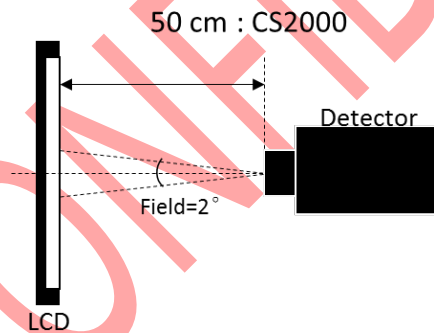


Fig.4.1 Measurement equipment.

4.2 Optical Specifications

The relative measurement methods of optical characteristics are shown in 4.2. The following items should be measured under the test conditions described in 4.1 and stable environment shown in 4.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity (CIE1931)	Red	Rx	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Angle at Normal Direction at center point of panel, Light source is HKC Backlight	Typ -0.03	0.637	Typ +0.03	-	(1)
		Ry			0.334			
	Green	Gx			0.299			
		Gy			0.642			
	Blue	Bx			0.152			
		By			0.063			
	White	Wx			0.280			
		Wy			0.308			
Color Gamut		DCI-P3	75	80	-	%	(2)	
Transmittance		T%	5.0	5.5	-	%	(3)	
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$	4000	5000	-	-	(4)
Response Time		T _g	With HKC BLU	-	8.5	19	ms	(5)
Viewing Angle	Horizontal	θ_{x+}	$CR \geq 10$ $\theta_x=0^\circ, \theta_y=0^\circ$	80	89	-	Deg.	(6)
		θ_{x-}		80	89	-		
	Vertical	θ_{y+}		80	89	-		
		θ_{y-}		80	89	-		
Gamma		γ	-	2.2	-	-	(7)	

Note:

Light source here is the backlight of HKC Module, and film structure is two DOP sheets.

- (1) Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying (Red, Green, Blue, White) and light source is defined by HKC Backlight, measurements shall be made at the center of the panel, and setup of measurement is shown in Fig 4.1.
- (2) The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1931 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig 4.1.
- (3) Definition of Transmittance (T%):

The transmittance is measured with full white pattern (L_{max}) at the center of the LCD panel.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}}$$

(4) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression,

$$\text{Contrast Ratio (CR): } CR = \frac{CR_W}{CR_D}$$

CR_W : Luminance of LCD module with full screen white pattern (255,255, 255) at center point.

CR_D : Luminance of LCD module with full screen Dark pattern (0, 0, 0) at center point.

Where the measure point of to the Contrast Ratio is the center of the panel

(5) Definition of Response time (Tg):

Average of gray to gray response time (T_g) means the average switching time of luminance ratios among 0%,25%,50%,75%,and 100% to each other and is optimized on frame rate =60Hz.

Measured Response time		To				
		0%	25%	50%	75%	100%
From	0%		$T_{0\%to25\%}$	$T_{0\%to50\%}$	$T_{0\%to75\%}$	$T_{0\%to100\%}$
	25%	$T_{25\%to0\%}$		$T_{25\%to50\%}$	$T_{25\%to75\%}$	$T_{25\%to100\%}$
	50%	$T_{50\%to0\%}$	$T_{50\%to25\%}$		$T_{50\%to75\%}$	$T_{50\%to100\%}$
	75%	$T_{75\%to0\%}$	$T_{75\%to25\%}$	$T_{75\%to50\%}$		$T_{75\%to100\%}$
	100%	$T_{100\%to0\%}$	$T_{100\%to25\%}$	$T_{100\%to50\%}$	$T_{100\%to75\%}$	

Table 4.2 Switching time of luminance ratios matrix

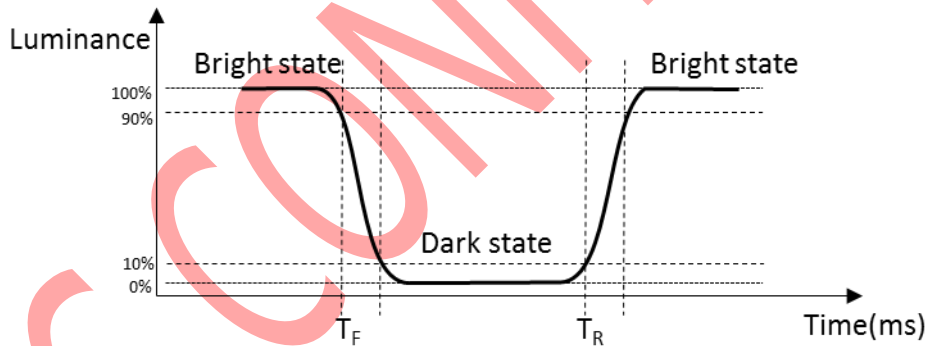


Fig 4.3 The definition of TR and TF

Measured response time is determined by 10% to 90% brightness difference of rising (T_R) or falling (T_F) time.

(6) Definition of Viewing angle:

As Note (4) the static contrast ratio definition, the viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the HKC's module (two vertical angles: up θ_y+ and down θ_y- ; and two horizontal angles: right θ_x+ and left θ_x-). The standard setup of measurement is shown in Fig 4.1 & 4.4

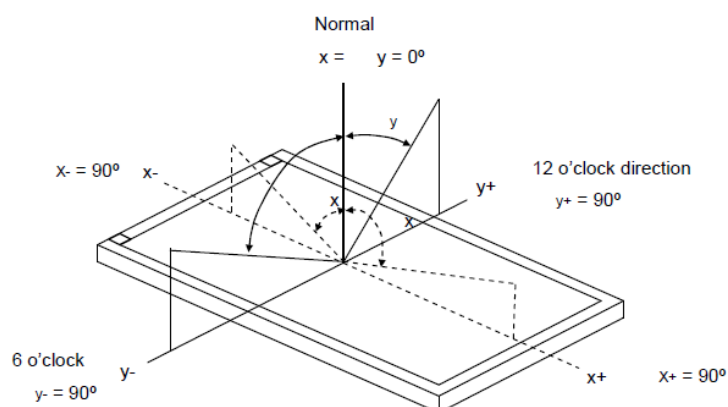


Fig 4.4 Definition of Viewing angle

(7) The gamma scale specification as shown in Table4.5:

Gray Level	Luminance(%) (Typ.)
L0	0.01
L15	0.22
L31	1.07
L47	2.60
L63	4.86
L79	7.86
L95	11.73
L111	16.41
L127	21.89
L143	28.51
L159	36.06
L175	44.53
L191	53.91
L207	64.24
L223	75.36
L239	87.63
L255	100.00

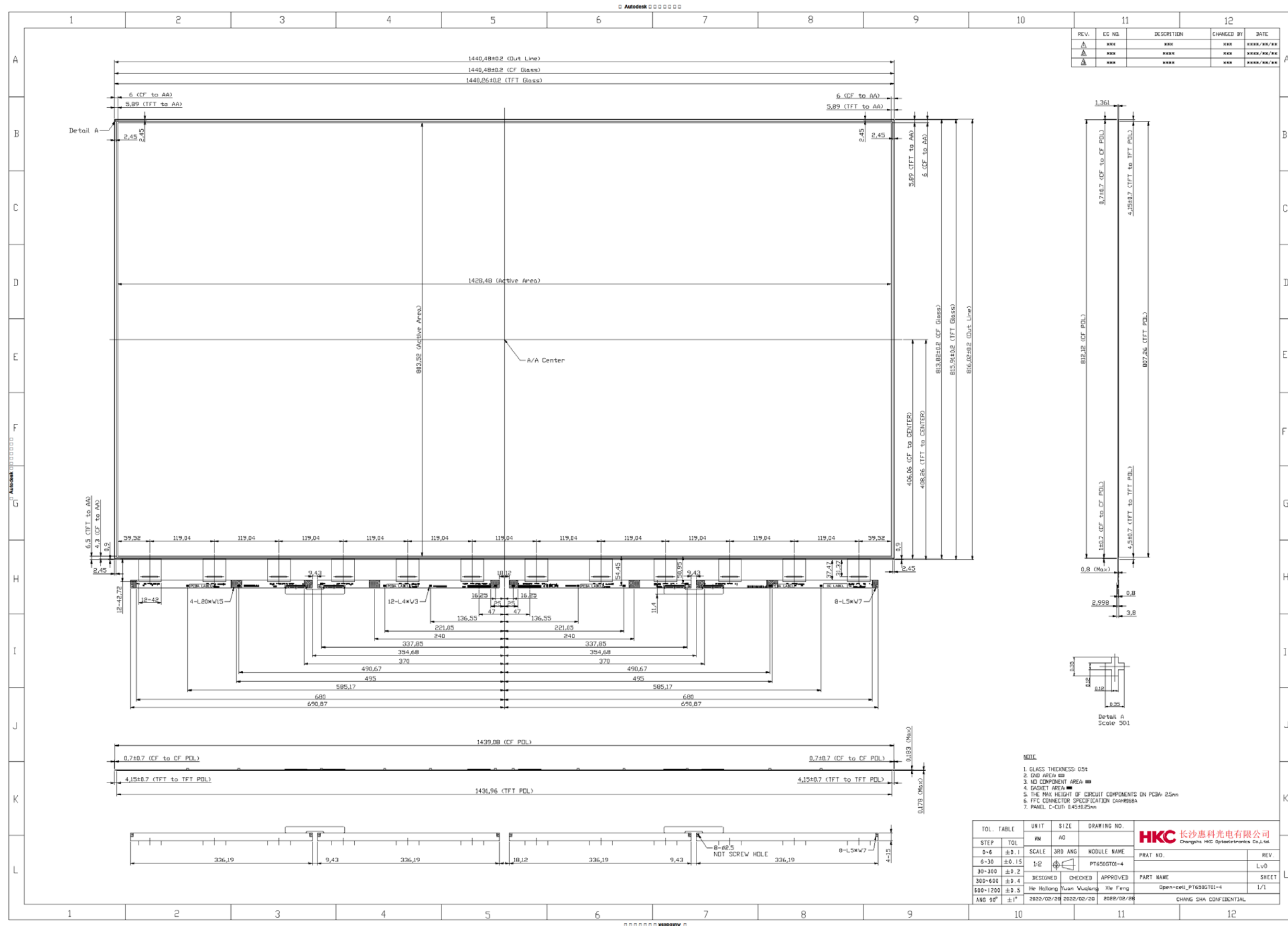
Table 4.5 Gray Scale Specification

5. MECHANICAL CHARACTERISTICS

Item	Specification	Unit	Note
Cell Outline Dimension	1440.48(H) x 816.02(V) x 1.361(D)	mm	D: cell thickness
Active area	1428.48(H) x 803.52(V)	mm	
Weight	3.31	Kg	
Surface Treatment	Type=AG	-	-
	Haze=3%		
	Top surface Hardness:3H	-	

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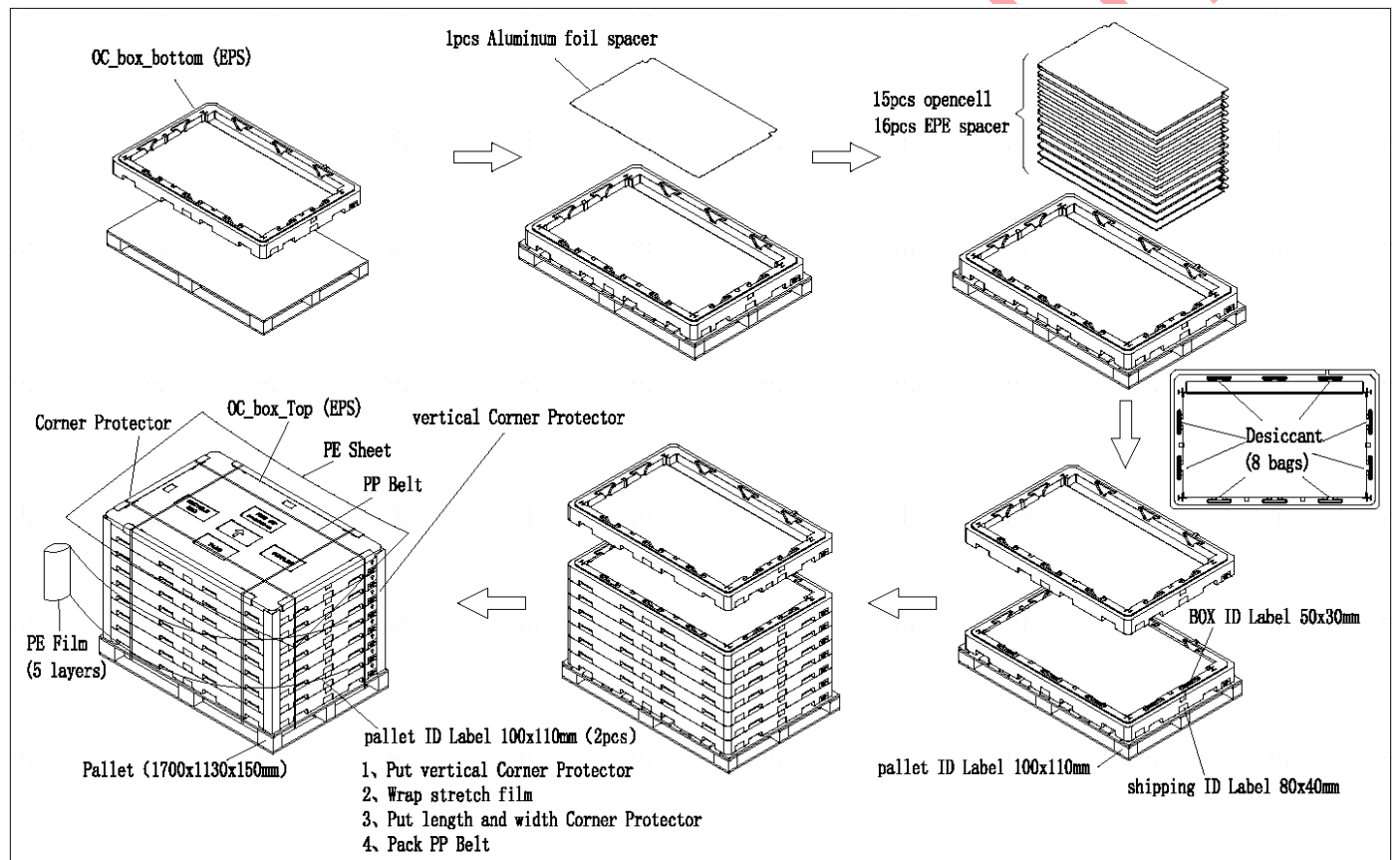
5.1 Mechanical Specification



5.2 Packing

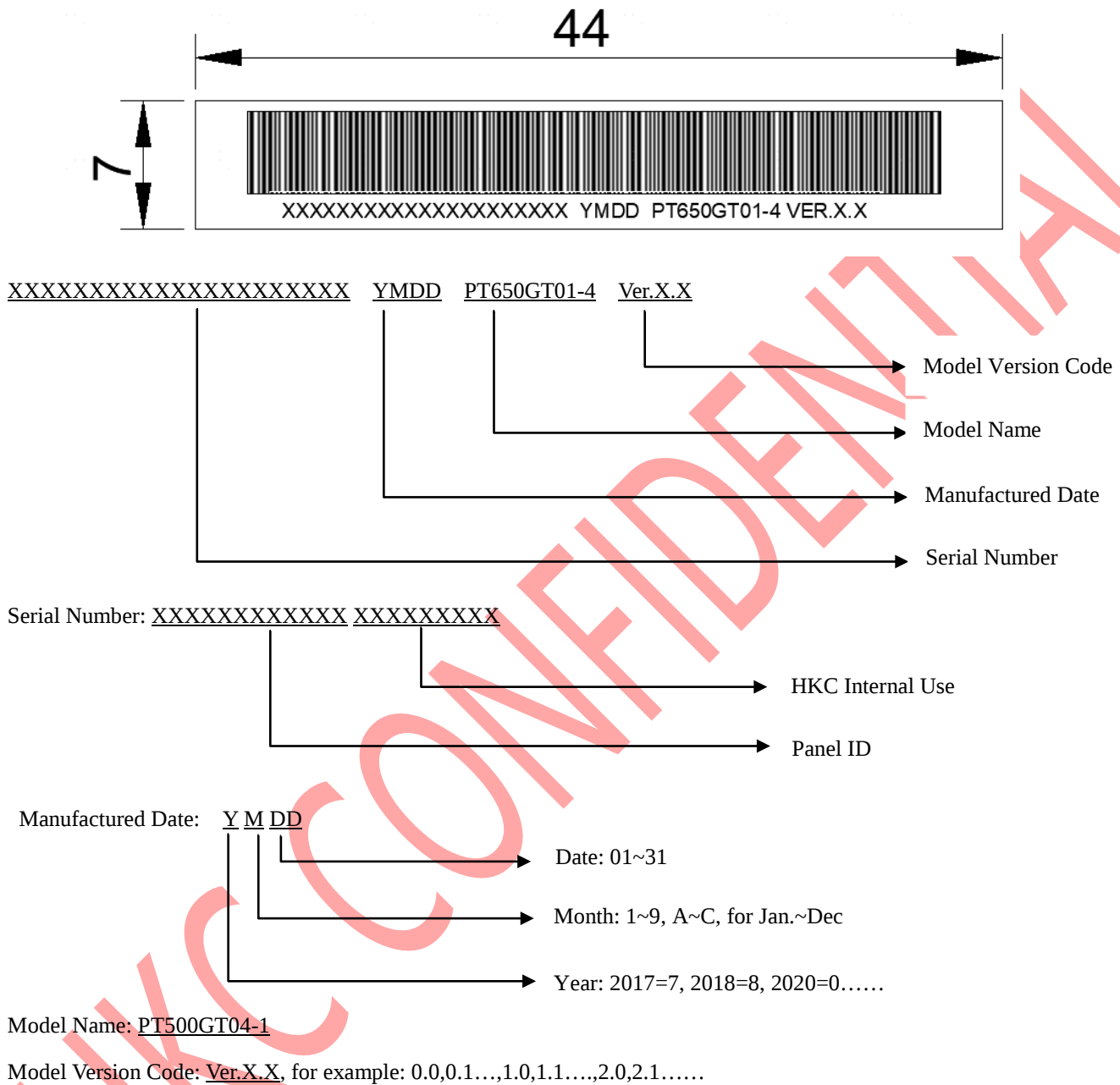
5.2.1 Packing Specifications

Item	Specification			
	Quantity	Dimension(mm)	Item	Weight(Kg)
Packing Box	15pcs/box	1655×1100×135	Net Weight	49.7
			Gross Weight	56.7
Pallet	1	1700×1130×150	Net Weight	28
Stack Layer	8			
Boxes per Pallet	8			
Pallet after Packing	120pcs/pallet	1700×1130×1190	Gross Weight	484.0

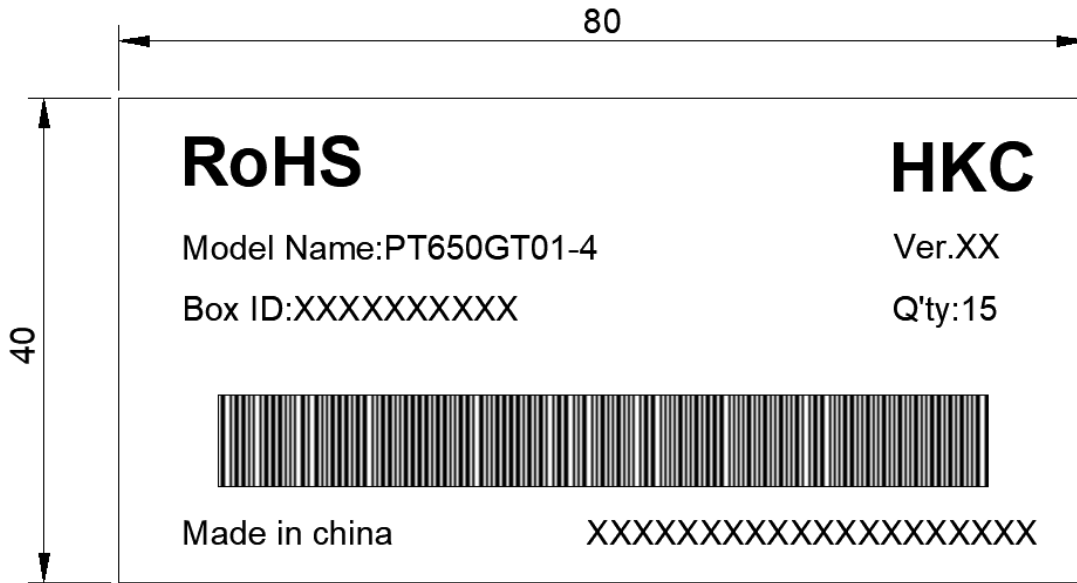


6. DEFINITION OF LABELS

6.1 Open Cell Label



6.2 Carton Label



Serial Number: XXXXXXXX XX XXXX XXXXXX



Box ID: XX XXX XXXXX

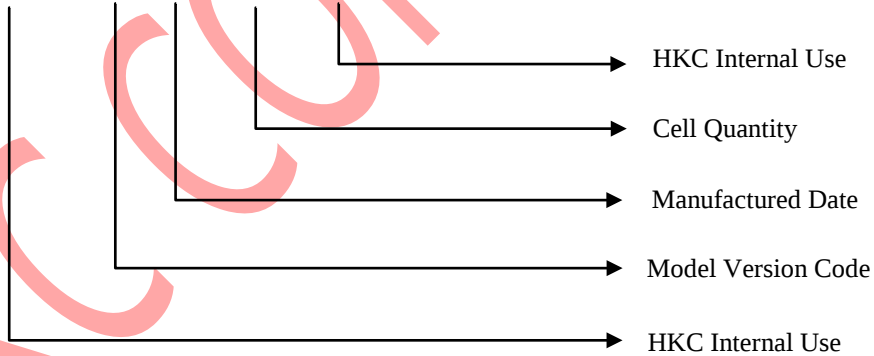


Model VersionCode: Ver.X.X, forexample:0.0,0.1...,1.0,1.1...,2.0,2.1.....

6.3 Pallet Label



Serial Number: XXXXXXXXXX XX XXXX XXXX XXXXXX



Pallet ID: XXXXXXXXXX

7. PRECAUTION

Please pay attention to the followings when a TFT-LCD cell is used, handled and mounted.

7.1 Unpacking

Should use immediately after unpacking TFT -LCD cell to prevent the terminal corrosion.

Protection film for a polarizer on a TFT open cell should be slowly peeled off so that the electrostatic charge can be minimized.

Source PCB should be connected to the ground when peel off the protection film.

The protection film should not be contacted to the driver during peeling off.

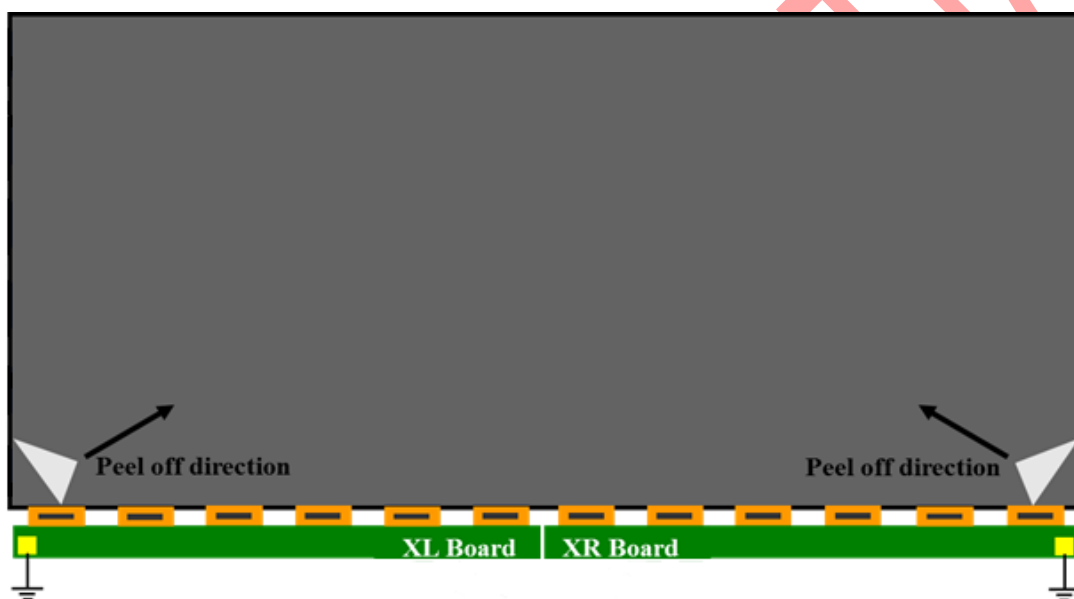


Fig 7.1 Unpacking

7.2 Storage Test

Any attachment on polarizer of open-cell, such as tape, is forbidden and not recommended, especially under the high temperature and high humidity environment.

8. GP REQUIREMENT

- a) RoHS, Directive 2011/65/EU of the European Parliament and council of 1 July 2011
- b) RoHS, Directive (EU) 2015/863 of the European Parliament and council of 31 March 2015
- c) PPW, Directive 94/62/EC on packaging and packaging waste with amendment (EU) 2018/852