Model name: PT430GT01-5

Date: 12. Nov. 2020

( ) Preliminary Specification

(√) Final Specification

Any modification is not allowed without HKC's permission

Customer's Approval	Chuzhou HKC
Approved by Company(公司): _____ Title(职称): _____ Signature(签名): _____	Approved By Product Director Date Name: Brian Signature: Brian 2020, 11, 14 Reviewed By PM Manager Date Name:Ella Signature: Ella 2020/11/12
Note	Reviewed By Project Leader Date Name:David Signature: David 2020/11/12 Reviewed By PM Date Name:Fang.Yang Signature: Fang.Yang 2020/11/12

Content

Revision History

Version	Date	Page (New)	Section	Description	Revision by
P1	2020/6/9	All	All	Preliminary Specification was First Issued.	Fang.Yang
P2	2020/7/28	P5 P8	1.1 3.1.1	Update General specifications Update Power consumption	Fang.Yang
P3	2020/9/2	P6	2.2	Update Absolute Ratings Of Environment	Fang .Yang
F1	2020/9/22	P12 P12	3.1.4 3.1.5	Add the operation temperature Add the setting date of theCEDS Eye Diagram	Fang .Yang
F2	2020/11/12	P30	5.1	Update Mechanical Specification	Fang .Yang

1. GENERAL DESCRIPTION

The specification is applied to 43” model (PT430GT01-5) TFT Liquid Crystal Display open cell and it supports 3840*2160 UD mode with 16.78M (8bit) colors. This product is with data driver ICs and two 68-pins connectors with CEDS interface on each left and right S-PCB without built-in backlight unit.

1.1 General Specifications

Item	Specification	Unit	Note
Screen Size	43 inch Diagonal	inch	-
Outline Dimension	953(H) × 543(V)	mm	D: cell thickness
Active area	941.184(H) × 529.416(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Cell transmittance	4.6(Typ.)	%	Clight，center point
Pixel Number	3840 × 2160	pixel	-
Sub Pixel Pitch	0.2451(H) × 0.2451(V)	mm	-
Pixel Arrangement	RGB vertical Island	-	-
Display Colors	16.78M	color	8bit
Display Mode	Normally Black	-	-
Display Orientation	Signal input with “ABC”	-	-
Panel Inversion Type	Column inversion	-	-
Surface Treatment	Type=AG	-	-
	Haze=3%		
	Top Surface Hardness : 3H	-	
Weight	1628	g	

Note:

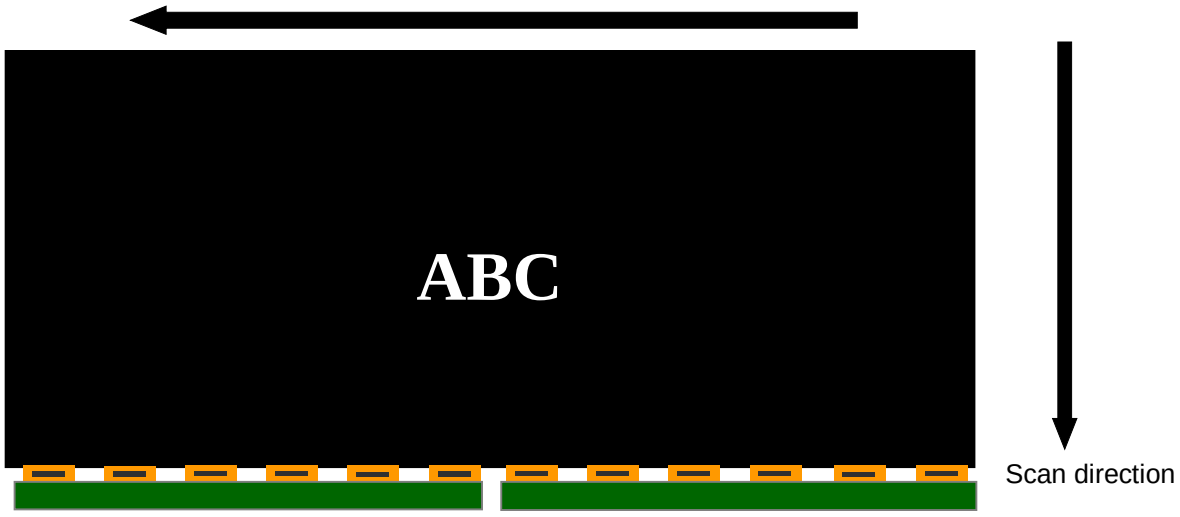


Fig 1.1 Display Orientation

2. ABSOLUTE MAXIMUM RATINGS

2.1 Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Demura_3.3V	V_{IN}	-0.3	3.6	V	
VCC18	V_{IN}	-0.3	2.5	V	
VDD	V_{IN}	-0.3	20.0	V	

2.2 Absolute Ratings of Environment

Temperature and relative humidity range is shown in the figure below.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	60	°C	(1)
Operating Temperature	TOP	0	50	°C	(1), (2)
Panel Surface Temperature of Display Area	PST	-	65	°C	(3)

Note:

(1) a. 90 % RH Max. (Ta ≤ 40 °C).

b. Web-bulb temperature should be 39℃ Max.(Ta>40℃)

c. No condensation

d. Operating condition with a assemble module

(2) Any point on the Driver surface must be less than 120 ºC under any condition ,If the surface temperature is out of the spec, thermal solutions should be applied to avoid be damaged.

(3) Surface temperature of display area is measured at 50℃ dry condition.

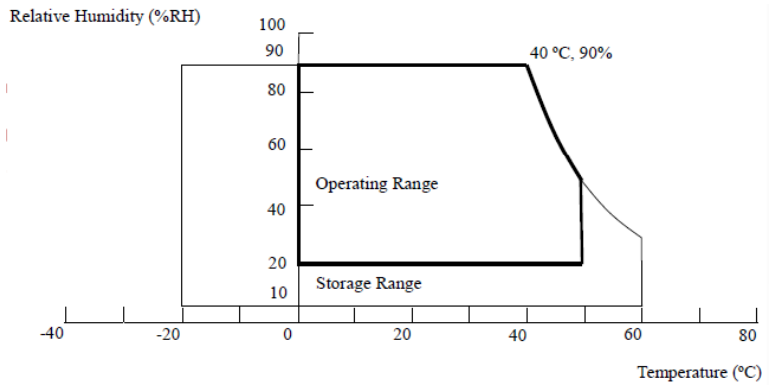


Fig. 2.1 Operating and Storage Environment

2.3 Package Storage

When storing open cell as spares for a long time, please follow the precaution instructions:

(1) Do not store the open cell in high temperature and high humidity for a long time. It is highly recommended to store the module with temperature from 20ºC to 30ºC in normal humidity (50 ± 10%RH) with shipping package.

(2) The open cell should be keep within one month shelf life.

3. ELECTRICAL SPECIFICATIONS

3.1 Electrical Characteristics

3.1.1 Power consumption

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Analog power for SD-IC		VDD	15.8	16.1	16.4	V	
Analog power for SD-IC		HVDD	7.03	7.23	7.43	V	
Digital power supply for SD-IC		VCC18	1.7	1.8	1.9	V	
Digital power for SD-IC		Vterm	1.1	1.2	1.3	V	
GDL high voltage		VGH (High level of CK、LC、STV)	29.2	30	30.8	V	（1）
GDL low voltage		VGL2 (Low level of CK、LC、STV)	-9.2	-8.9	-8.6	V	
		VGL1	-6.9	-6.6	-6.3	V	
Power for Common electrode		VCOM1	4.83	5.83	6.83	V	（2）
Digital power for demura		Demura_3.3V	3.0	3.3	3.6	V	
Gamma voltage		GMA1	13.85	14	14.15	V	
		GMA3	11.49	11.64	11.79	V	
		GMA5	10.35	10.5	10.65	V	
		GMA7	9.71	9.86	10.01	V	
		GMA9	7.34	7.49	7.64	V	
		GMA10	6.81	6.96	7.11	V	
		GMA12	4.56	4.71	4.86	V	
		GMA14	3.83	3.98	4.13	V	
		GMA16	2.56	2.71	2.86	V	
		GMA18	0.35	0.5	0.65	V	
Power Supply current	White Pattren	I_W	-	0.534	0.694	A	(3)
	Horizontal Stripe	I_H	-	1.207	1.569	A	
	Black Pattern	I_B	-	0.503	0.654	A	
	Mosanic 8*6	I_M	-	0.522	0.679	A	
Power consumption	White Pattren	P_W	-	7.05	9.17	W	
	Horizontal Stripe	P_H	-	15.94	20.722	W	
	Black Pattern	P_B	-	6.64	8.64	W	

	Mosanic 8*6	P_M	-	6.89	8.96	W	

Note:

(1) Ambient temperature: 25 ± 2ºC .

(2) VCOM voltage depend on the flicker pattern's performance; VCOM adjustable range: min ~ max value.

(3) The measured data is based on Siliconworks' CB ver01（The consumption is CB ver 01+OC）

3.1.2 Power design current demand

Symbol	Max	Unit	Note
VDD	1100	mA	
HVDD	500	mA	
VCC18	200	mA	
Vterm	100	mA	
VGL1	50	mA	
VCOM1	100	mA	
VDD3V3	20	mA	
GMA1	30	mA	
GMA3	30	mA	
GMA5	30	mA	
GMA7	30	mA	
GMA9	30	mA	
GMA10	30	mA	
GMA12	30	mA	
GMA14	30	mA	
GMA16	30	mA	
GMA18	30	mA	

3.1.3 Max power noise

Parameter	Symbol	Max	Unit	Note
Power Supply Voltage	VCC18	50	mV	
	Vterm	50	mV	
	VDD3V3	100	mV	
	VGL1	150	mV	
	VCOM1	150	mV	
	HVDD	200	mV	
	VDD	500	mV	
	GMA1	150	mV	
	GMA3	150	mV	
	GMA5	150	mV	
	GMA7	150	mV	
	GMA9	150	mV	
	GMA10	150	mV	
	GMA12	150	mV	
	GMA14	150	mV	
	GMA16	150	mV	
	GMA18	150	mV	

3.1.4 CEDS Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Units
Modulation Ratio of SSC	t11	Modulation freq. = 100kHz	-1	-	1	%
		Modulation freq. = 50kHz	-2	-	2	%
Internal Termination Resistor	RT	TA=25℃	Typ.-20%	50	Typ.+20%	Ω
Modulation Frequency of SSC	t12	Max. modulation rate = 1%	-	-	100	KHz
CEDS input differential voltage	VID	VCCA,D=1.62~1.98V	150	-	500	mV
CEDS input center voltage	VIB	VCCA,D=1.62~1.98V	-	VTERM-VID/2	-	V
TERM Voltage	VTERM	VCCA,D=1.62~1.98V	0.9	-	1.4	V

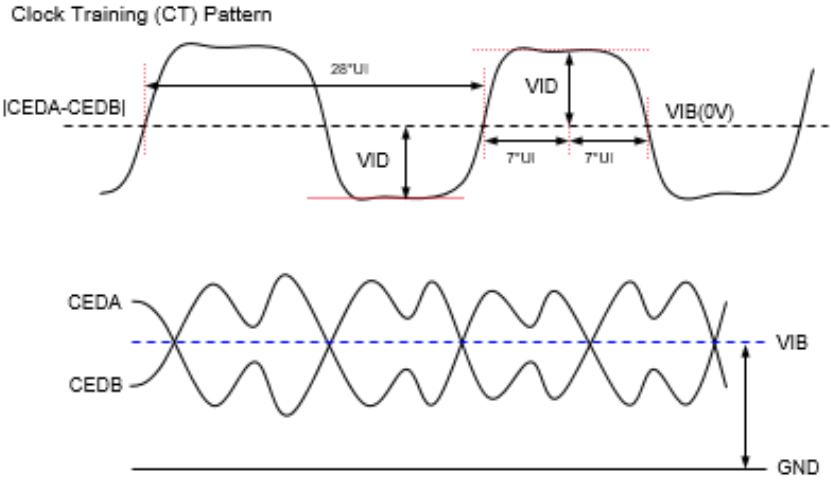


Fig. 3.1 CEDS signal definition

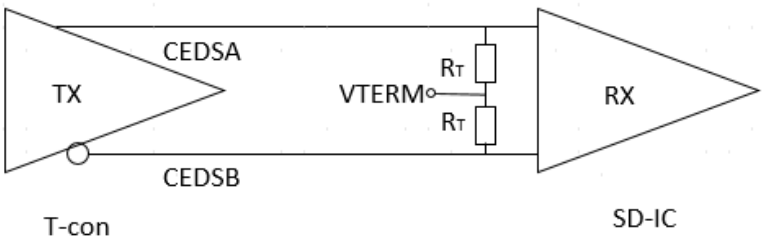


Fig. 3.2 Internal Termination Resistor

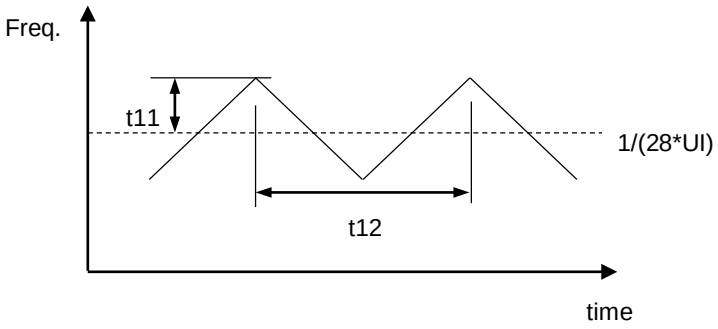


Fig. 3.3 SSCG modulation by modulating clock period

3.1.5 CEDS Eye Diagram

Parameter	Symbol	Condition	Min	Typ	Max	Units	Note
Effective Veye level[1,2)]	VEYE	VCCA,D=1.62~1.98V	75	-	-	mV	（1）
Unit interval (UI)[1,2)]	t	1.62V ≤ VCC ≤ 1.98V	0.65	-	0.83	ns	
Eye-Open time[1,2)]	t2-1, t2-2	1.62V ≤ VCC ≤ 1.98V	0.25	-	-	UI	

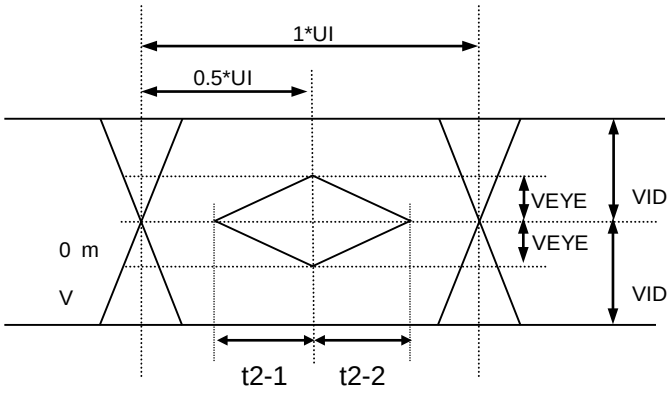


Fig. 3.4 CEDS Eye Diagram

(1)Eye-diagram measurement conditions：

a.PLL type=2nd PLL; Loop Bandwidth=5MHz; Damping factor=0.7G（Default）; SSC=OFF;

Real Time=Disable DSP(@Tektronix)

b.Accumulated Number of UIs=At least 1 Frame Data(≒27,000,000 UI @UHD)；

c.The test temperature is 0-50 ℃.

3.2 Interface Connections

3.2.1 Interface Pin Assignment

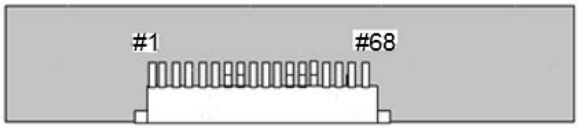
XL			XR		
Pin No.	**Symbol**	**Description**	**Pin No.**	**Symbol**	**Description**
1	GMA18	Gamma voltage	1	GOA_CLK1	Clock input for GDL circuit
2	GMA16	Gamma voltage	2	GOA_CLK2	Clock input for GDL circuit
3	GMA14	Gamma voltage	3	GOA_CLK3	Clock input for GDL circuit
4	GMA12	Gamma voltage	4	GOA_CLK4	Clock input for GDL circuit
5	GMA10	Gamma voltage	5	GOA_CLK5	Clock input for GDL circuit
6	GMA9	Gamma voltage	6	GOA_CLK6	Clock input for GDL circuit
7	GMA7	Gamma voltage	7	GOA_CLK7	Clock input for GDL circuit
8	GMA5	Gamma voltage	8	GOA_CLK8	Clock input for GDL circuit
9	GMA3	Gamma voltage	9	NC	Not connection
10	GMA1	Gamma voltage	10	NC	Not connection
11	GND	Ground	11	GND	Ground
12	NC	Not connection	12	LC2	Low frequency clock
13	NC	Not connection	13	LC1	Low frequency clock
14	NC	Not connection	14	VGL1	Power supply for GDL power
15	NC	Not connection	15	GOA_RESET	Power supply for GDL power
16	NC	Not connection	16	STV	Start pulse for GDL power
17	NC	Not connection	17	VGL2	Power supply for GDL power
18	NC	Not connection	18	NC	Not connection
19	LOCK_SOC	Lock signal for source IC	19	NC	Not connection
20	GND	Ground	20	VCOM1	Power supply for VCOM
21	DATA6N	CEDS data 6-	21	VDD	Power supply for analog circuit
22	DATA6P	CEDS data 6+	22	VDD	Power supply for analog circuit
23	GND	Ground	23	VDD	Power supply for analog circuit
24	DATA5N	CEDS data 5-	24	VDD	Power supply for analog circuit
25	DATA5P	CEDS data 5+	25	VDD	Power supply for analog circuit
26	GND	Ground	26	HVDD	Power supply for analog circuit
27	DATA4N	CEDS data 4-	27	VCC18	Power supply for digital circuit
28	DATA4P	CEDS data 4+	28	VCC18	Power supply for digital circuit
29	GND	Ground	29	VCC12	Power supply for digital circuit
30	DATA3N	CEDS data 3-	30	LOCK_MODULE	Lock signal for source IC

31	DATA3P	CEDS data 3+	31	GND	Ground
32	GND	Ground	32	DATA12N	CEDS data 12-
33	DATA2N	CEDS data 2-	33	DATA12P	CEDS data 12+
34	DATA2P	CEDS data 2+	34	GND	Ground
35	GND	Ground	35	DATA11N	CEDS data 11-
36	DATA1N	CEDS data 1-	36	DATA11P	CEDS data 11+
37	DATA1P	CEDS data 1+	37	GND	Ground
38	GND	Ground	38	DATA10N	CEDS data 10-
39	LOCK_MODULE	Lock signal for source IC	39	DATA10P	CEDS data 10+
40	VCC12	Power supply for digital circuit	40	GND	Ground
41	VCC18	Power supply for digital circuit	41	DATA9N	CEDS data 9-
42	VCC18	Power supply for digital circuit	42	DATA9P	CEDS data 9+
43	HVDD	Power supply for analog circuit	43	GND	Ground
44	VDD	Power supply for analog circuit	44	DATA8N	CEDS data 8-
45	VDD	Power supply for analog circuit	45	DATA8P	CEDS data 8+
46	VDD	Power supply for analog circuit	46	GND	Ground
47	VDD	Power supply for analog circuit	47	DATA7N	CEDS data 7-
48	VDD	Power supply for analog circuit	48	DATA7P	CEDS data 7+
49	VCOM1	Power supply for VCOM	49	GND	Ground
50	NC	Not connection	50	NC	Not connection
51	NC	Not connection	51	GMA18	Gamma voltage
52	VGL2	Power supply for GDL power	52	GMA16	Gamma voltage
53	STV	Start pulse for GDL power	53	GMA14	Gamma voltage
54	GOA_RESET	Power supply for GDL circuit	54	GMA12	Gamma voltage

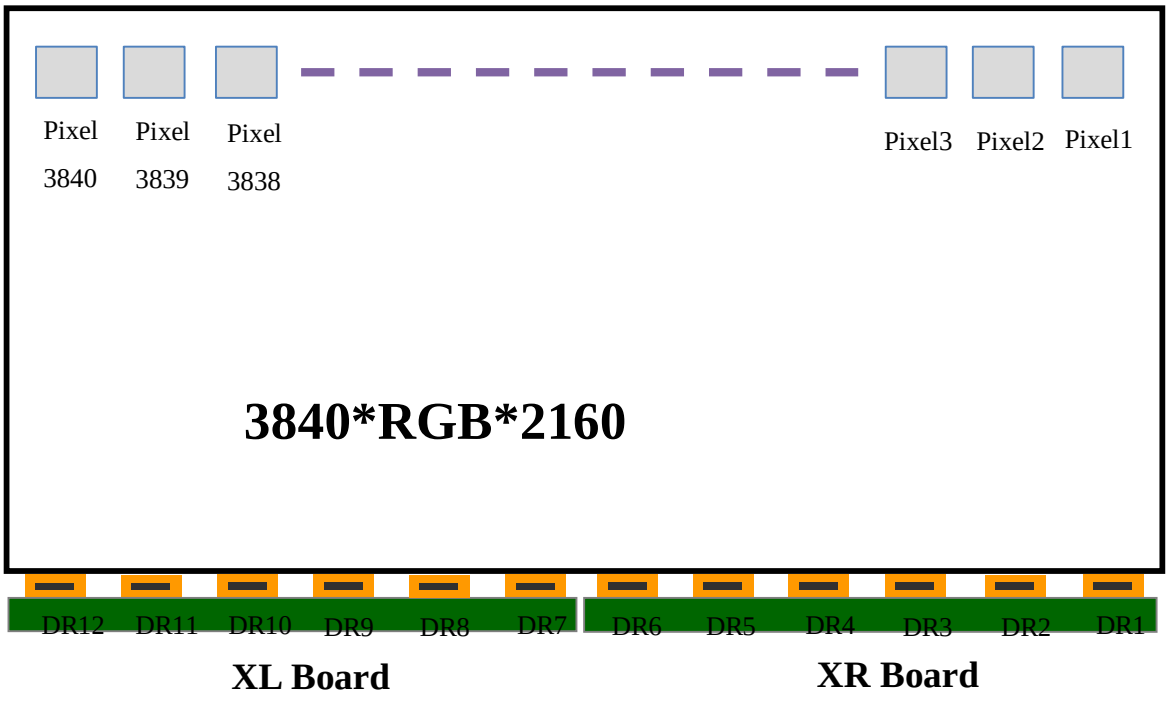
55	VGL1	Power supply for GDL circuit		55	GMA10	Gamma voltage
56	LC1	Low frequency clock		56	GMA9	Gamma voltage
57	LC2	Low frequency clock		57	GMA7	Gamma voltage
58	GND	Ground		58	GMA5	Gamma voltage
59	NC	Not connection		59	GMA3	Gamma voltage
60	NC	Not connection		60	GMA1	Gamma voltage
61	GOA_CLK8	Clock input for GDL circuit		61	WP	Write protect signal
62	GOA_CLK7	Clock input for GDL circuit		62	Demura_MISO	SPI Data input
63	GOA_CLK6	Clock input for GDL circuit		63	GND	Ground
64	GOA_CLK5	Clock input for GDL circuit		64	Demura_CS	Chip select
65	GOA_CLK4	Clock input for GDL circuit		65	Demura_MOSI	SPI Data output
66	GOA_CLK3	Clock input for GDL circuit		66	GND	Ground
67	GOA_CLK2	Clock input for GDL circuit		67	Demura_CLK	Clock signal
68	GOA_CLK1	Clock input for GDL circuit		68	Demura_3.3V	Logic Voltage 3.3V

Note:

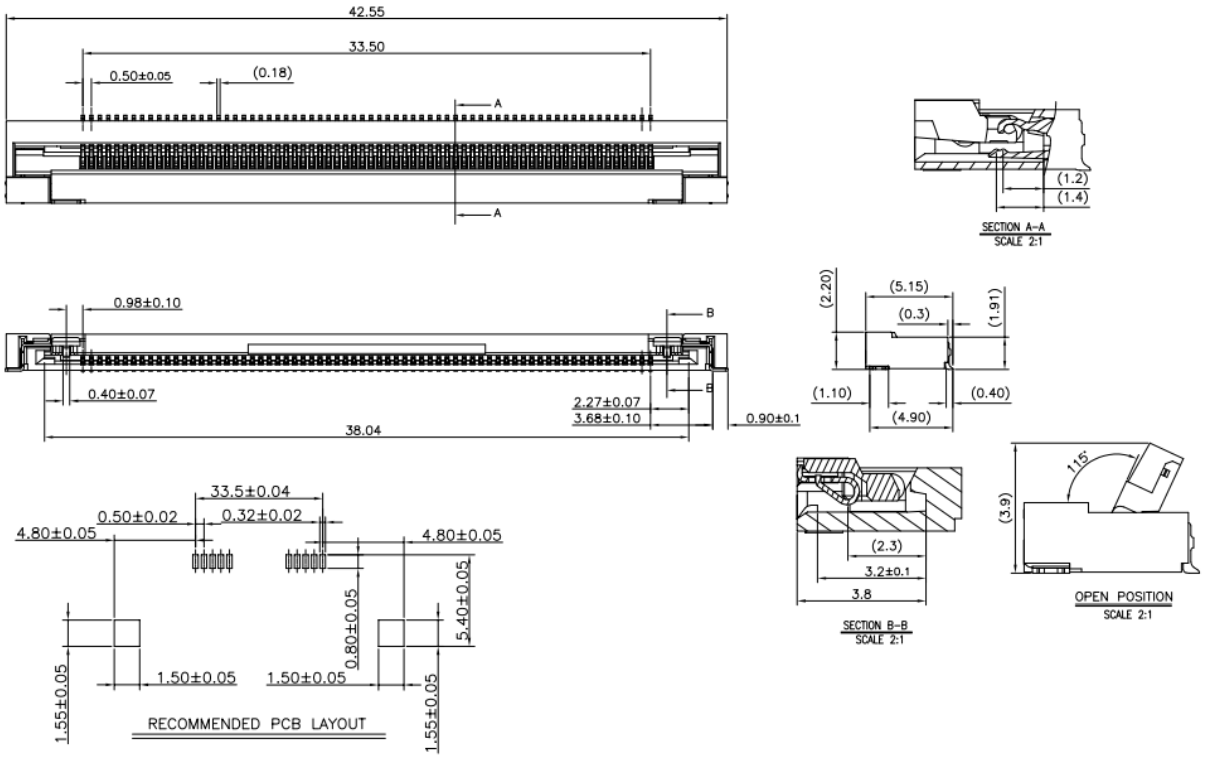
1）The input connector is CAAHR068A (Tranit) or the same specification of other vendor，pin one is on left



2） Diagram of interface

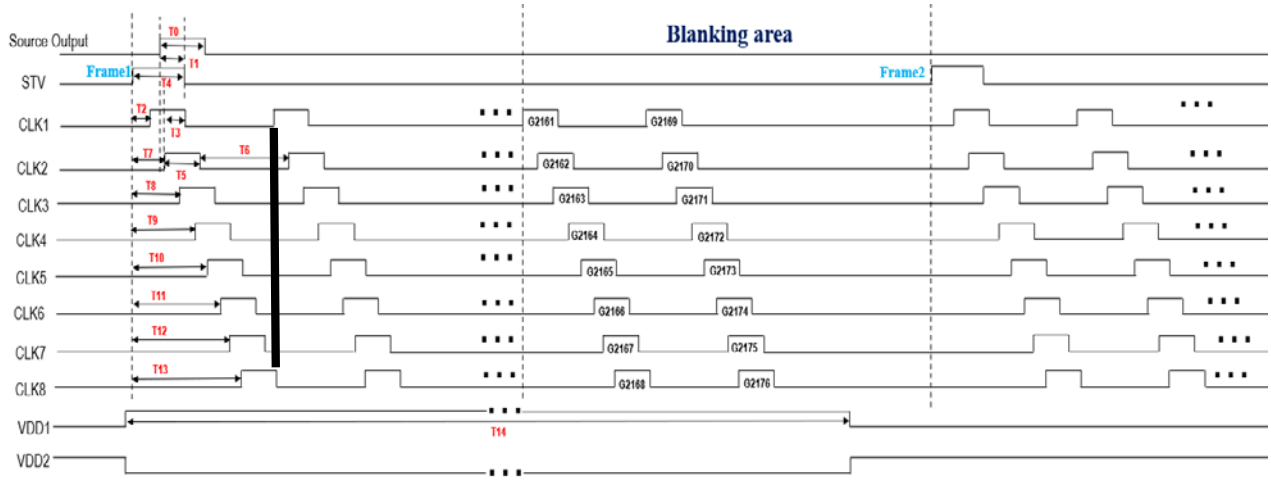


3.2.2 Mechanism drawings



3.3 Timing Spec.

This timing Spec is design value, which may be adjusted according to the actual situation in the future.



Timing	Description	Spec
T0	Data width	1H
T1	Data output to CK1 falling	4.4us
T2	STV rising to CK1 rising	2H
T3	CK2 rising to CK1 falling	5H/3
T4	STV Width	14H/3
T5	CKV Width	8H/3
T6	CKV Low	16H/3
T7	STV rising to CK2 rising	3H
T8	STV rising to CK3 rising	4H
T9	STV rising to CK4rising	5H
T10	STV rising to CK5 rising	6H
T11	STV rising to CK6 rising	7H
T12	STV rising to CK7 rising	8H
T13	STV rising to CK8 rising	9H
T14	LC change width (high 50%=low 50%)	100frame
N	CKV number of 1 frame	272

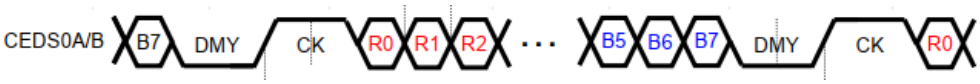
Condition：Frame rate=60Hz，V-total=2250，H-total=4400

3.4 Source Driver Data Mapping & Setting

3.4.1 CEDS data mapping

DR NO.	Data Channel NO.				
DR1	1	2	3	……	961
DR2	962	963	964	……	1921
DR3	1922	1923	1924	……	2881
DR4	2882	2883	2884	……	3841
DR5	3842	3843	3844	……	4801
DR6	4802	4803	4804	……	5761
DR7	5762	5763	5764	……	6721
DR8	6722	6723	6724	……	7681
DR9	7682	7683	7684	……	8641
DR10	8642	8643	8644	……	9601
DR11	9602	9603	9604	……	10561
DR12	10562	10563	10564	……	11521

8bit signal-1pair



Output	Out1	Out2	Out3	Out4	Out5	Out6	Out7	Out8	Out9
Order	1st data			2th data			3th data		
Data	R1[0]-R1[7]	G1[0]-G1[7]	B1[0]-B1[7]	R2[0]-R2[7]	G2[0]-G2[7]	B2[0]-B2[7]	R3[0]-R3[7]	G3[0]-G3[7]	B3[0]-B3[7]
→	Out958	Out959	Out960	Out961	Out962	Out963	Out964	Out965	Out966
→	320th data			321th data			322th data		
→	R320[0]-R320 [7]	G320 [0]-G320 [7]	B320 [0]-B320 [7]	R321[0]-R321[7]	G321[0]-G321 [7]	B321[0]-B321 [7]	R322[0]-R322[7]	G322[0]-G322 [7]	B322 [0]-B322 [7]

3.4.2 CEDS Command & REG Setting

Control data pockets & setting

-	Bit No	Packet Name	Setting value	Remarks
CTRS	0,1	CK	11	
	2	CTRS[0]	0	Indicates the packet is the control packet LLLLLL
	3	CTRS[1]	0	
	4	CTRS[2]	0	
	5	CTRS[3]	0	
	6	CTRS[4]	0	
	7	CTRS[5]	0	
	8	POL	0 ↔ 1	Toggle every frame, Polarity control bit.
	9	GSP	-	Gate Start Pulse
	10	CS1	0	Operated Charge Share mode when output polarity changed
	11	TESTC[0]	0	Internal Test Mode User should fix these bits to “LL” level.
	12	TESTC[1]	0	
	13	H6INV	0	Polarity control bit.
	14	POL2	0 ↔ 1	Toggle every frame, Polarity control bit.
	15	TESTD	0	Internal Test Mode
	16	H2POL	0	H2POL = “L” : Normal POL; H2POL = “H” : POL inversion
	17	TESTE[0]	0	Internal Test Mode
	18	TESTE[1]	0	
	19	CS0	0	Operated Charge Share mode when output polarity changed
	20	SLEW1	1	Normal Power Mode(75%)
	21	SLEW0	0	
	22	HPOL	0	Polarity control bit.
	23	TESTA[1]	0	Test mode TESTA[1] = “L” : Normal Mode TESTA[1] = “H” : SOE Monitoring Test Mode User should be fix this bit to “L” level.

	24	TESTA[2]	0	Internal Test Mode User should fix these bits to “LL” level.
	25	TESTA[3]	0	
	26~27	DMY	00	-

-	Bit No	Packet Name	LCM setting Value		Remarks
			SD-ICs @ SEL1/0=LH	SD-IC @ SEL1/0=LL	
CTR1	0,1	CK	11		
	2	SOE_S[0]	1		SOE Start packet data (311) →SOE Start time = First data + 314PCLK SOE Pulse Width = 404ns@1.386Gbps
	3	SOE_S[1]	1		
	4	SOE_S[2]	1		
	5	SOE_S[3]	0		
	6	SOE_S[4]	1		
	7	SOE_S[5]	1		
	8	SOE_S[6]	0		
	9	SOE_S[7]	0		
	10	SOE_S[8]	1		
	11	SOE_S[9]	0		
	12	SOE_E[0]	0	0	SOE End packet data (10) for 960ch mode → SOE End time = Last data + 14PCLK SOE End packet data(8) for 966ch mode → SOE End time = Last data + 12PCLK Note: You need to subtract 2 from the current SOE End packet value for chips with SEL1/0=”LL” applied.
	13	SOE_E[1]	1	0	
	14	SOE_E[2]	0	0	
	15	SOE_E[3]	1	1	
	16	SOE_E[4]	0	0	
	17	SOE_E[5]	0	0	
	18	SOE_E[6]	0	0	
	19	SOE_E[7]	0	0	
	20	D_SCR_EN	1		Data scramble function
	21		1		
	22		1		

	23	D_SCR_RST	1	
	24		1	
	25		1	
	26~27	DMY	0 0	

3.5 Power On/Off Sequence

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.

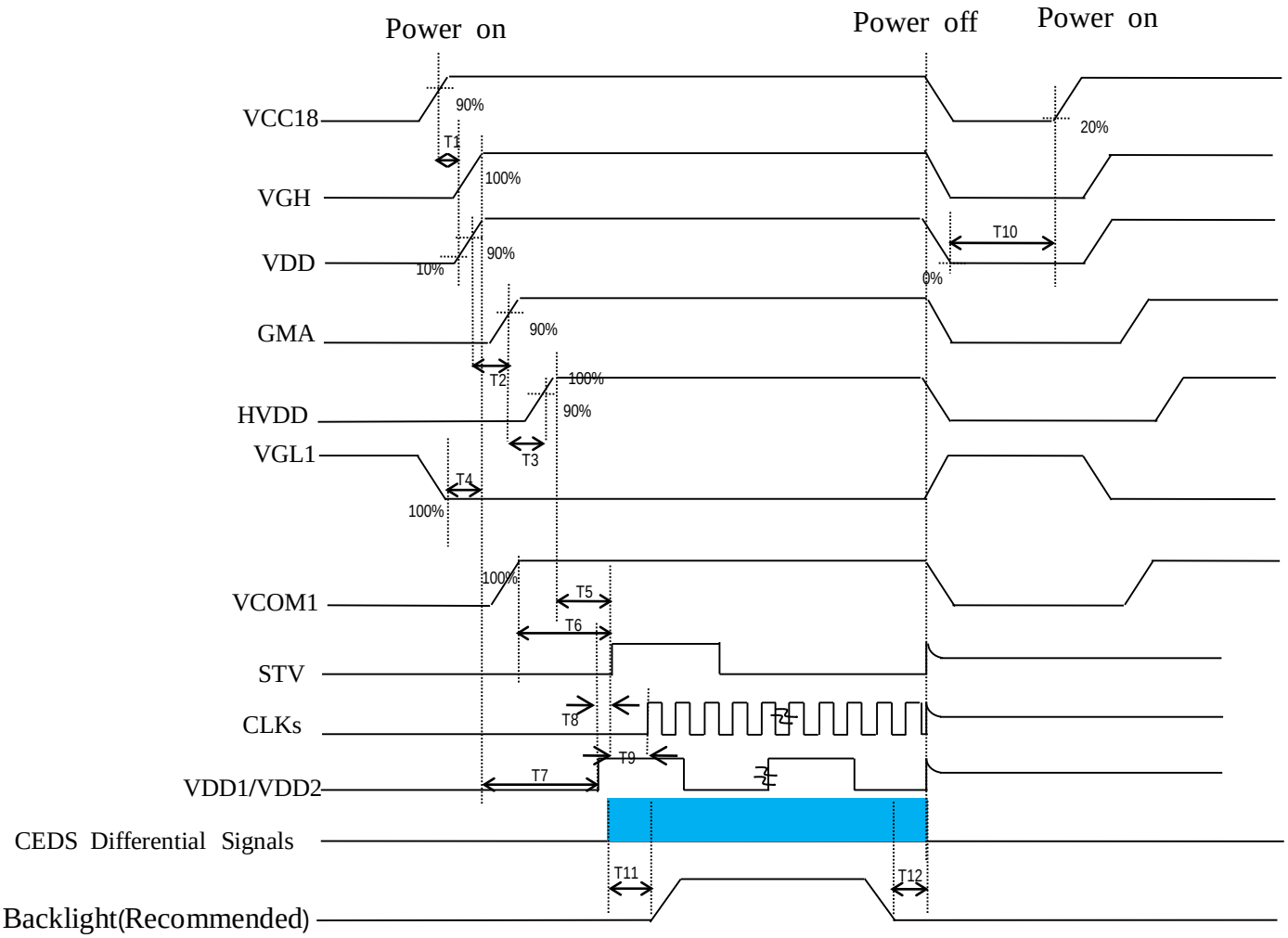


Fig. 3.1 Power on/off sequence

Parameters	Values			Units
	Min.	Typ.	Max.	
T1	>0	-	-	ms
T2	>0	-	-	ms
T3	-200	-	1000	ms
T4	>0	-	-	ms
T5	>0	-	-	ms
T6	>0	-	-	ms
T7	>0	-	-	ms
T8	>0	-	-	ms
T9	-	14.82		us
T10	1000			ms
T11	20			ms
T12	20			ms

Attention:

(1) Apply the light bar voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(2) Before power on, please keep the level of input signals on the low or high impedance.

(3) T11 should be measured after the module has been fully discharged between power off and on period.

(4) Interface signal shall not be kept at high impedance when the power is on.

(5) The product should be always operated within above ranges.

(6) VDD must be higher than gamma voltage all the time.

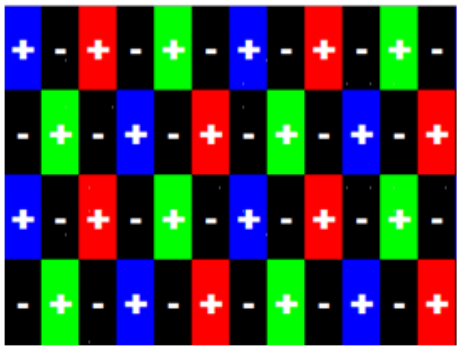
(7) CEDS signals must be transmitted continuously during power on condition，and the SOC is recommended to insert at least one frame black pattern before power off.

(8) All GDL signals pull up to VGH when power off.

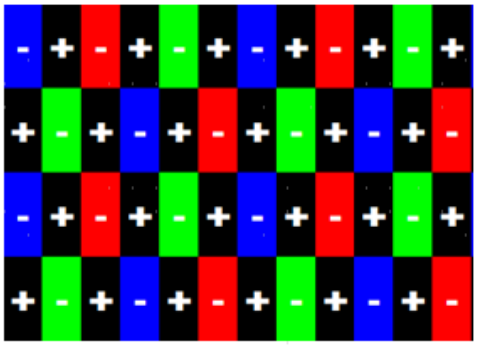
3.6 Flicker Adjustment

Flicker must be optimized after module assembly and aging. Its patterns are as follow:

Frame N



Frame N+1



Bright sub-pixel=G127(50% grayscale); dark sub-pixel=G0（0%grayscale）

Fig 3.2 Flicker pattern

3.7 Driver IC ESD Spec

If the LCD module is designed with the Plastic Bezel, we suggest ESD protection solutions should be applied to avoid IC damaged, as shown in Fig.3.3.

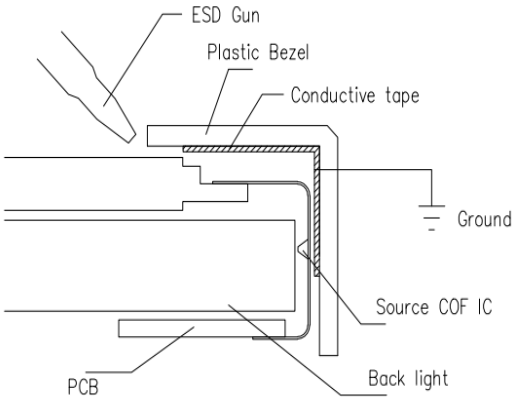


Fig. 3.3 Source COF IC ESD protection

4. OPTICAL CHARACTERISTICS

4.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25±2	ºC
Ambient Humidity	H_A	50±10	% RH
Supply Voltage	V_{CC}	12	V
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Vertical Refresh Rate	F_v	60	Hz
Light source	HKC module White LED Backlight Module/ Film structure		
Warm up time	Twarm	>30 min	min
Dark room	ED	1lux>	lux

To avoid abrupt temperature change during optical measurement, the measurement should be executed in a stable, windless，in dark room after lighting the light source.

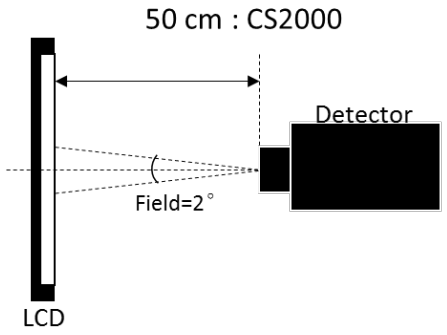


Fig.4.1 Measurement equipment.

4.2 Optical Specifications

The relative measurement methods of optical characteristics are shown in 4.2. The following items should be measured under the test conditions described in 4.1 and stable environment shown in 4.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity (CIE1931)	Red	Rx	θ_x=0°,θ_y=0° Viewing Angle at Normal Direction at center point of panel, Light source is C-light	Typ - 0.03	(0.661)	Typ + 0.03	-	(1)
		Ry			(0.326)			
	Green	Gx			(0.278)			
		Gy			(0.591)			
	Blue	Bx			(0.136)			
		By			(0.096)			
	White	Wx			(0.314)			
		Wy			(0.357)			
Color Gamut		CG		-	72	-	%	(2)
Transmittance		T%		-	4.6	-	%	(3)
Contrast Ratio		CR	θ_x=0°,θ_y=0° With HKC Backlight	-	5000	-	-	(4)
Response Time		T_g		-	9.5	19	ms	(5)
Viewing Angle	Horizontal	θ_x+	CR≧10	-	89	-	Deg.	(6)
		θ_x -		-	89	-		
	Vertical	θ_y+		-	89	-		
		θ_y-		-	89	-		

Note:

Light source here is the backlight of HKC BLU and film structure is two diffuser sheets

(1) Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying (Red, Green, Blue, White) and light source is defined by C-light, Measurements shall be made at the center of the panel, and setup of measurement is shown in Fig.4.1.

(2) The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1931 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig.4.1.

(3) Definition of Transmittance (T%):

The transmittance is measured with full white pattern (L_{max}) at the center of the LCD panel.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}}$$

(4) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression,

Contrast Ratio (CR): $\boldsymbol{CR = \frac{CR_W}{CR_D}}$

CRW: Luminance of LCD module with full screen white pattern (255, 255, 255) at center point.

CRD: Luminance of LCD module with full screen Dark pattern (0, 0, 0) at center point.

Where the measure point of to the Contrast Ratio is the center of the panel

(5) Definition of Response time (Tg):

Average of gray to gray response time (Tg) means the average switching time of luminance ratios among 0%,25%,50%,75%,and 100% to each other and is optimized on frame rate =60Hz.

Measured Response time		To				
		0%	25%	50%	75%	100%
From	0%		$T_{0\%to25\%}$	$T_{0\% \text{ to } 50\%}$	$T_{0\% \text{ to } 75\%}$	$T_{0\% \text{ to } 100\%}$
	25%	$T_{25\% \text{ to } 0\%}$		$T_{25\% \text{ to } 50\%}$	$T_{25\% \text{ to } 75\%}$	$T_{25\% \text{ to } 100\%}$
	50%	$T_{50\% \text{ to } 0\%}$	$T_{50\% \text{ to } 25\%}$		$T_{50\% \text{ to } 75\%}$	$T_{50\% \text{ to } 100\%}$
	75%	$T_{75\% \text{ to } 0\%}$	$T_{75\% \text{ to } 25\%}$	$T_{75\% \text{ to } 50\%}$		$T_{75\% \text{ to } 100\%}$
	100%	$T_{100\% \text{ to } 0\%}$	$T_{100\% \text{ to } 0\%}$	$T_{100\% \text{ to } 50\%}$	$T_{100\% \text{ to } 75\%}$	

Table.4.2 switching time of luminance ratios matrix

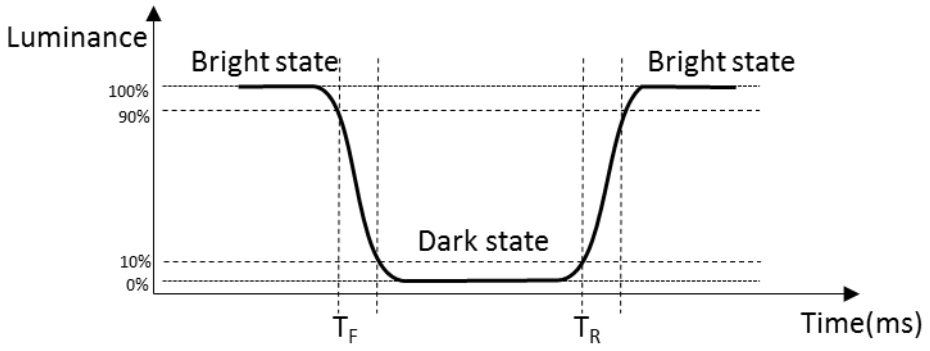


Fig.4.3 The definition of T_R and T_F

Measured response time is determined by 10% to 90% brightness difference of rising (T_R) or falling (T_F) time,

(6) Definition of Viewing angle:

As Note (4) the static contrast ratio definition, the viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the HKC's module (two vertical angles: up θ_y+ and down θ_y-; and two horizontal angles: right θ_x+ and left θ_x-). The standard setup of measurement is shown in Fig. 4.1 & 4.4.

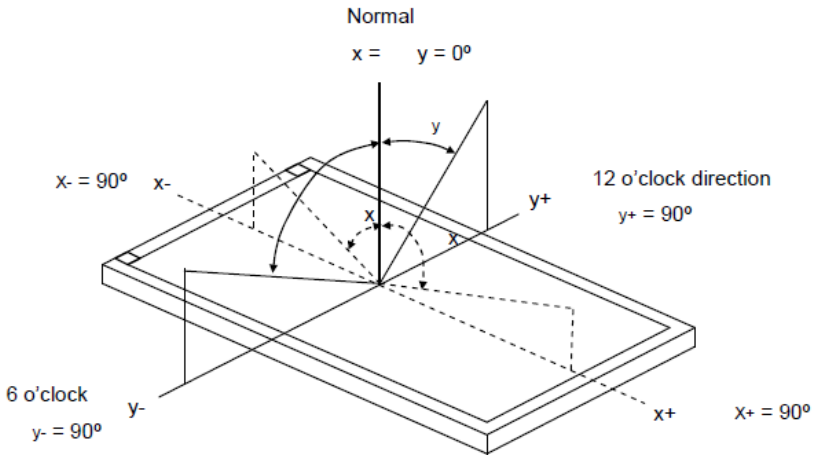


Fig.4.4 View angle coordination system

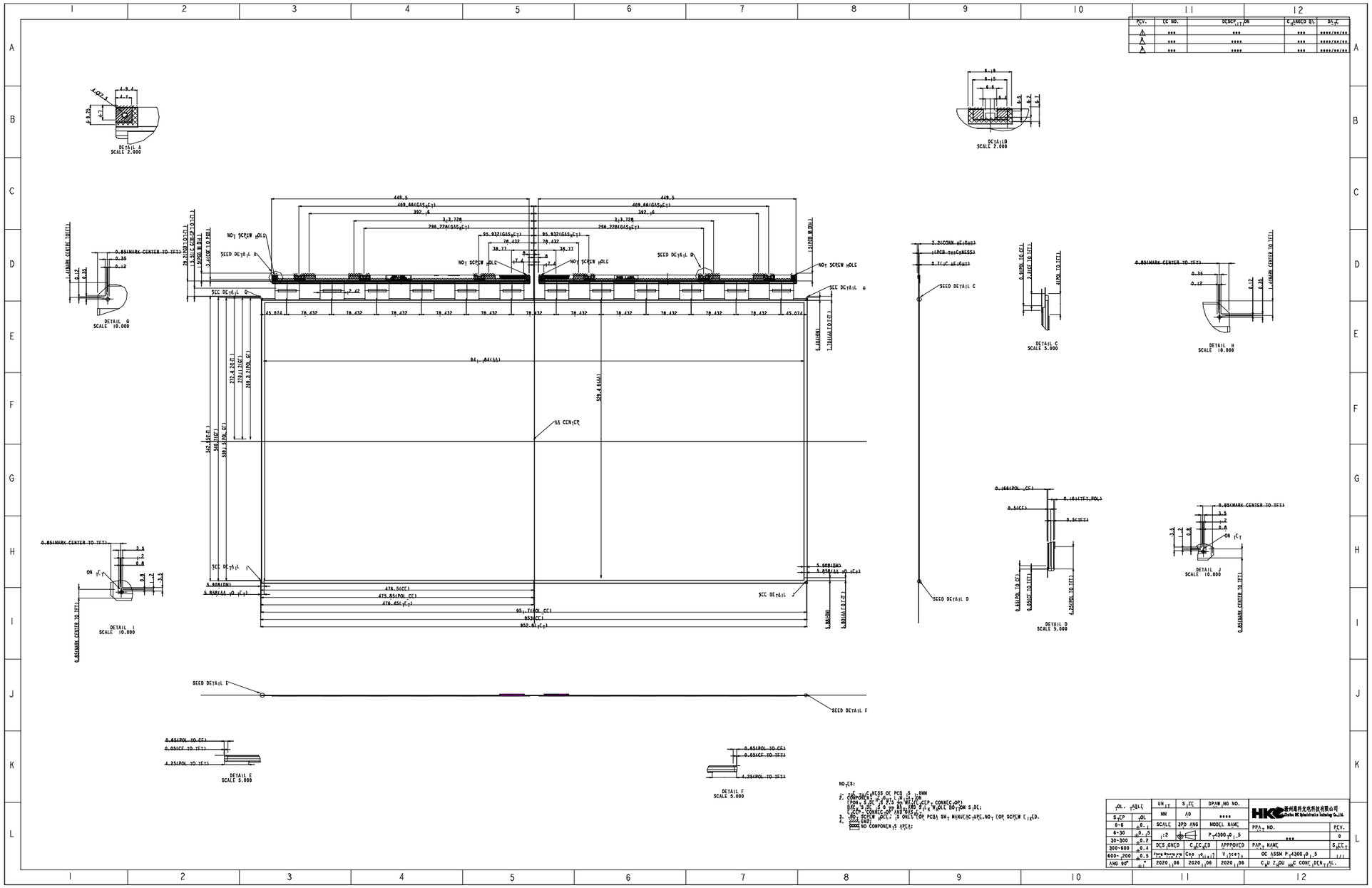
(7) The gamma scale specification as shown in Table 4.5.

Gray Level	Luminance [%] (Typ.)
L0	0.02
L15	0.20
L31	0.97
L47	2.42
L63	4.61
L79	7.59
L95	11.39
L111	16.04
L127	21.58
L143	28.01
L159	35.37
L175	43.68
L191	52.95
L207	63.20
L223	74.45
L239	86.71
L255	100

Table 4.5. Gray scale specification

5. MECHANICAL CHARACTERISTICS

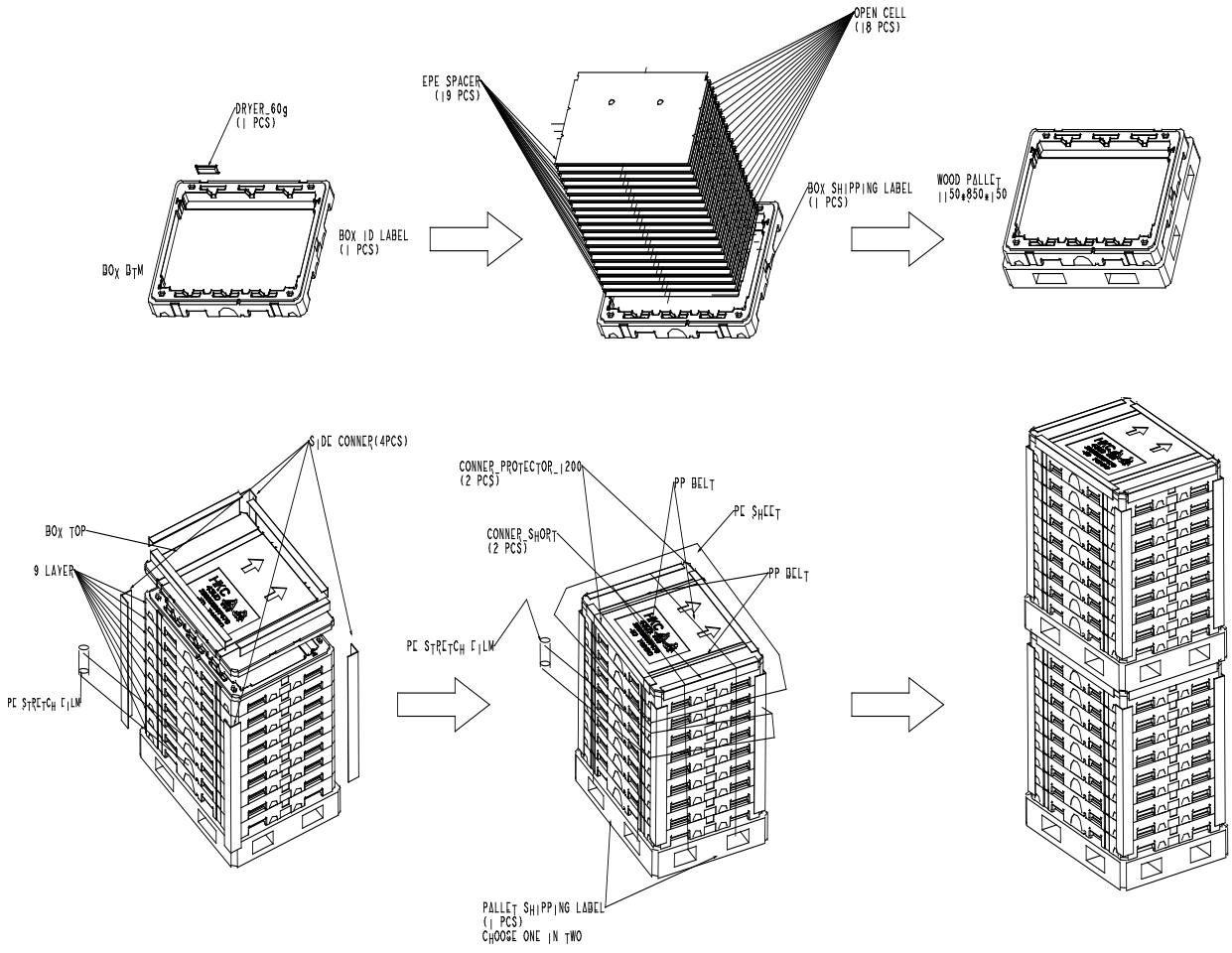
5.1 Mechanical Specification



5.2 Packing

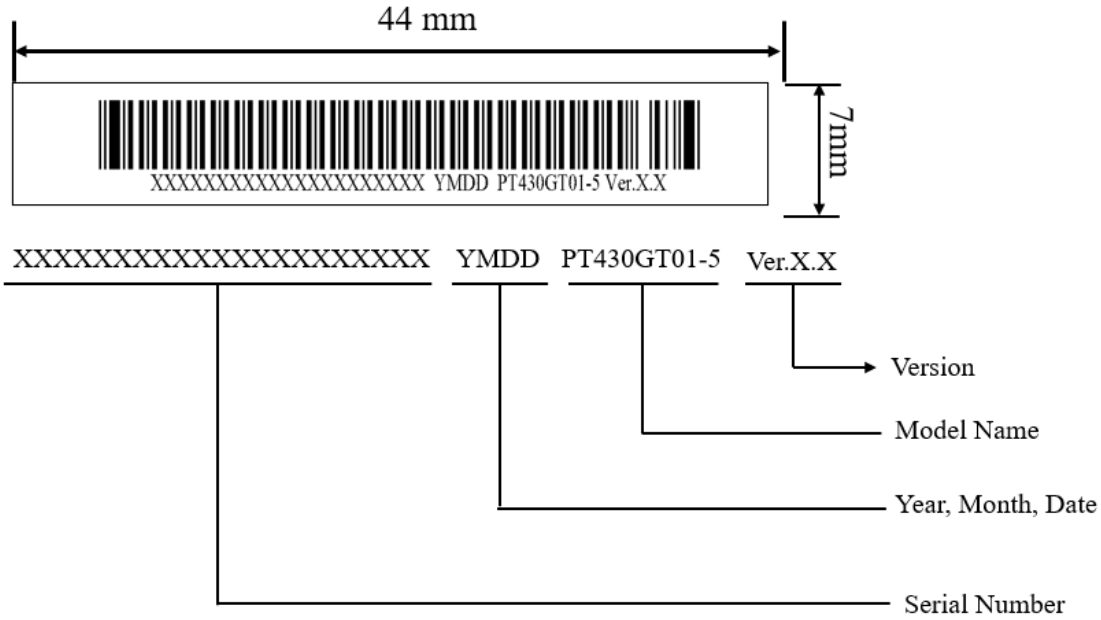
5.2.1 Packing Specifications

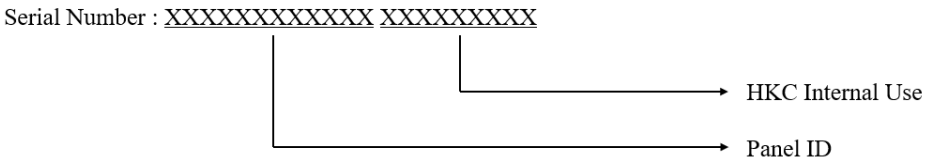
Item	Specification			
	Quantity	Dimension(mm)	Item	Weight(Kg)
Packing Box	18pcs/box	1100 × 800 × 108.5	Net Weight Gross Weight	29.3 32
Pallet	1	1150 × 850 ×150	Net Weight	14.8
Stack Layer	9			
Boxes per Pallet	9			
Pallet after Packing	162pcs/pallet	1150 × 850 ×1060.5	Gross Weight	299

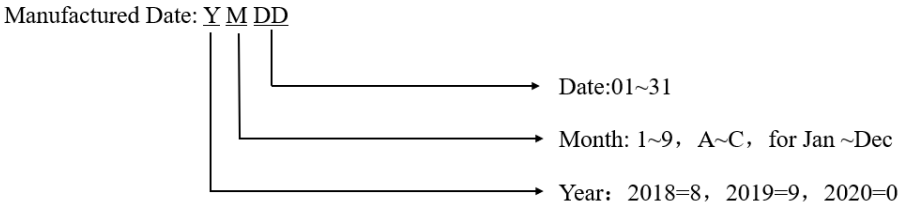


6. DEFINITION OF LABELS

6.1 Open Cell Label



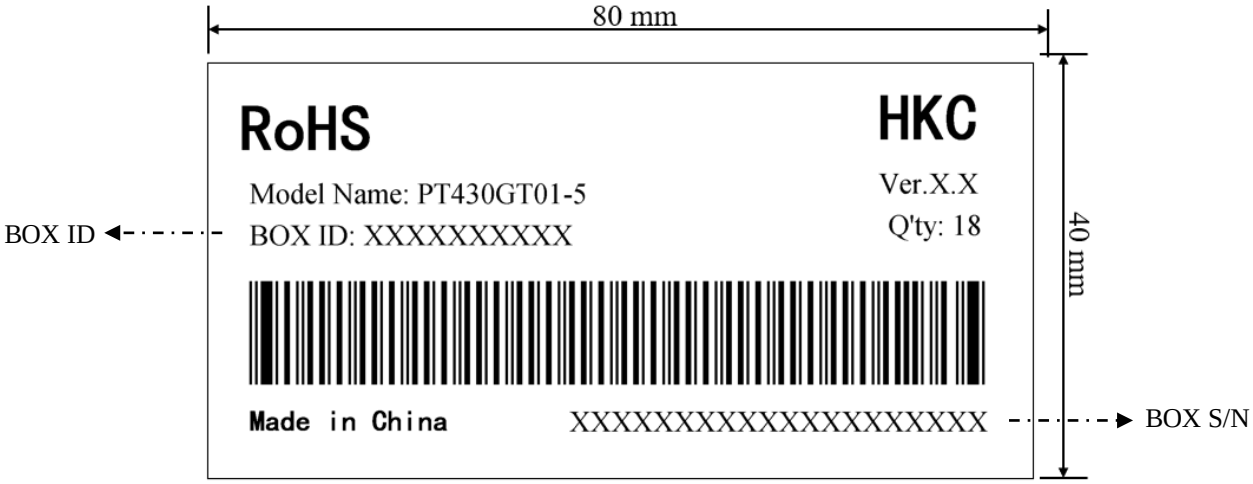


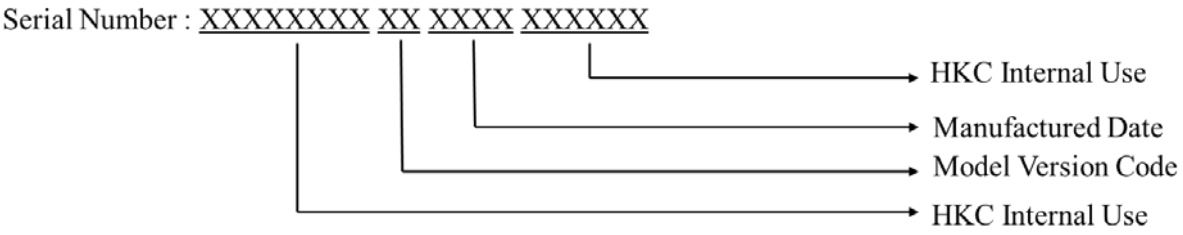


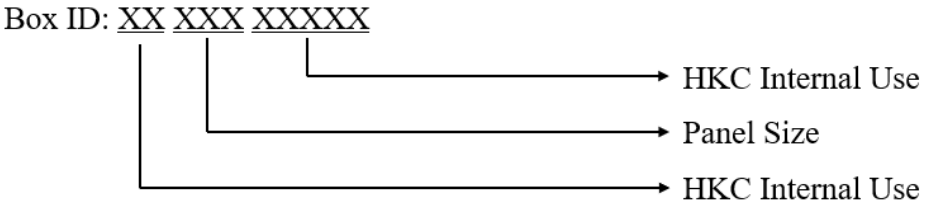
Model Name：PT430GT01-5

Model Version Code：Ver.X.X.，for example：0.0,0.1…，1.0,1.1…，2.0,2.1……

6.2 Carton Label

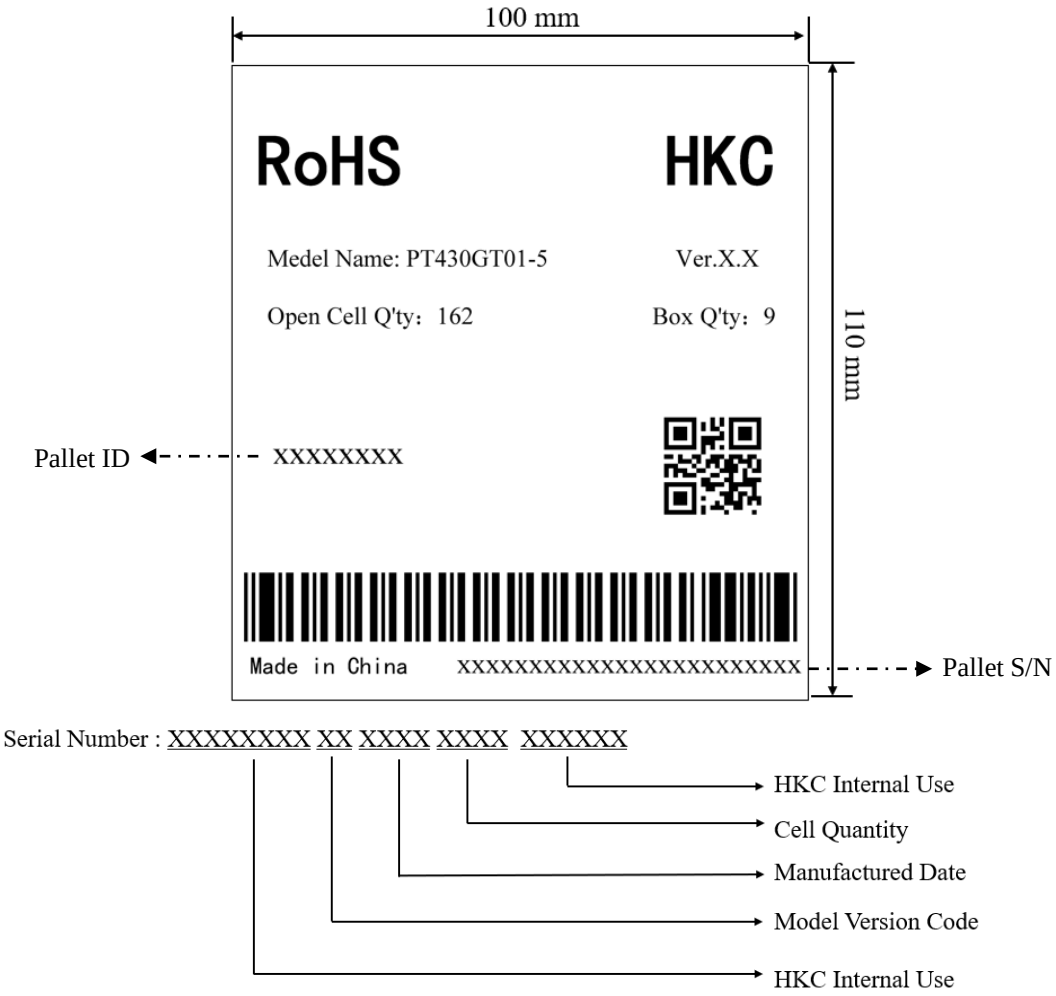






Model Version Code：Ver.X.X.，for example：0.0,0.1…，1.0,1.1…，2.0,2.1……

6.3 Pallet Label



7.RELIABILITY TEST ITEMS

	Test Items	Condition
1	High Temperature	50ºC, Operation; 240hrs
2	High Temperature	60ºC, Storage; 240hrs
3	Low Temperature	-5ºC, Operation; 240hrs
4	Low Temperature	-20ºC, Storage; 240hrs
5	High Temperature HighHumidity Operation	50ºC/80%RH, Operation; 240hrs
6	Thermal Shock	(-20ºC; 0.5hrs)=>(60ºC; 0.5hrs)]/cycle; 100cycles
7	Altitude Test Storage	RT, 193mbar(12000m/40000ft), Storage; 24hrs
8	On/Off Test	(RT, 10sec on, 5sec off)/cycle; 30000cycles
9	Image Sticking-1	(RT, Checkerboard 8x6; 1hr)=>(RT, check by middle gray-127th; in 3min)
10	Image Sticking-2	(RT, Cross Talk Pattern; Power 12hrs)=>Power Off; 12hrs=>(RT, check by middle gray-127th) gray-127th)
11	High Temperature High Humidity Storage	60ºC/90%RH, Storage; 240hrs
12	Packing Vibration-1	1.15Grms Random frequency 1~200Hz, 60min/Bottom, follow ISTA:1Hz(0.0001g2/Hz), 4Hz(0.01g2/Hz), 100Hz(0.01g2/Hz), 200Hz(0.001g2/Hz)
13	Packing Vibration-2	2.0Grms Random frequency 3~300Hz/(0.0144g2/Hz), 60min/Bottom

Note: Before and after reliability test, open cell should be with normal function.

8. PRECAUTION

Please pay attention to the followings when a TFT-LCD cell is used, handled and mounted.

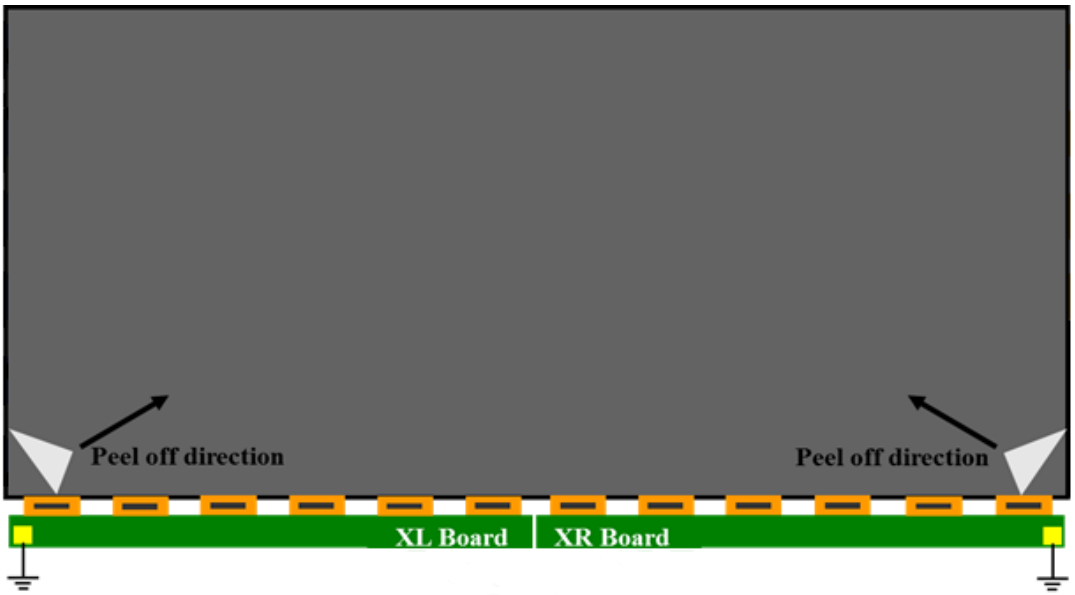
8.1 Unpacking

Should use immediately after unpacking TFT -LCD cell to prevent the terminal corrosion.

Protection film for a polarizer on a TFT open cell should be slowly peeled off so that the electrostatic charge can be minimized.

Source PCB should be connected to the ground when peel off the protection film.

The protection film should not be contacted to the driver during peeling off.



8.2 Storage test

Any attachment on polarizer of open-cell, such as tape, is forbidden and not recommend, especially under the high temperature and high humidity environment.

9. GP REQUIREMENT

a) RoHS, Directive 2011/65/EU of the European Parliament and council of 1 July 2011

b) RoHS, Directive (EU) 2015/863 of the European Parliament and council of 31 March 2015

c) PPW